Area Selective Deposition
Room ETEC Atrium - Session ASD1-TuM

ASD: Plasma, Selective Etching and Sustainability

Moderators: Han-Bo-Ram Lee, Incheon National University, **Marko Tuominen**, ASM

8:30am **ASD1-TuM-1 Versatile Strategies for ASD Optimization Using Super-Cycles***, **Marceline Bonvalot**, Martial Santorelli,* LTM - MINATEC - CEA/LETI, France*; Christophe Vallée,* SUNY College of Nanoscale Science and Engineering **INVITED**

As the semiconductor industry advances toward extreme miniaturization and 3D integration, transistor architectures are progressively evolving toward gate-all-around devices based on stacked nanosheet channels. In parallel, emerging complementary field effect transistor (CFET) technologies further extend this concept by vertically stacking n- and p-type channels on top of each other within the same device footprint. The fabrication of such highly integrated architectures puts stringent demands on thin film deposition processes, making the development of innovative atomic layer deposition (ALD) approaches increasingly critical, owing to intrinsic advantages, such as high conformality, excellent uniformity over large surface areas and precise control of film composition at relatively low temperatures. ALD also provides numerous opportunities for the selective and precise placement of materials (semiconductors, dielectrics and metals) with nanoscale thickness control on horizontal and/or vertical surfaces, thereby enabling simplified integrated fabrication flows. This presentation will discuss various process routes based on ABC super-cycle strategies to achieve selective growth in semiconducting device fabrication. Tailoring precursor sequencing and surface chemistry through controlled adsorption, ligand exchange, and surface termination will be addressed, in the light of precise control of nucleation and selectivity required in complex 3D features in the context of extreme miniaturization.

9:00am **ASD1-TuM-3 Self-Aligned Patterning by Area-Selective Etching of Polymers and Area-Selective Atomic Layer Deposition: Decreasing Polymer Flow and Activating Noncatalytic Surface***, **Valtteri Lasonen**, Piyumi Liyana Pathiranage, Mykhailo Chundak, Marko Vehkamäki,* University of Helsinki, Finland*; Matthias Carnoy, Benjamin Borie,* ATLANT 3D, Denmark*; Silvia Armini,* IMEC, Belgium*; Mikko Ritala,* University of Helsinki, Finland

Area-selective etching (ASE) of polymers is a novel self-aligned patterning technique.[1-3] Polymer patterning is achieved by catalytic decomposition of the polymer film only on top of catalytically active surfaces, whereas the polymer film stays intact on top of the noncatalytic surfaces. After the self-aligned patterning, area-selective deposition can be done using the patterned polymer as an inhibition layer.

Previously, we have demonstrated the feasibility of the ASE process with three polymers: MLD-polyimide[1], poly(methyl methacrylate) (PMMA)[2], and poly(lactic acid) (PLA)[3] – using Pt as the catalytic surface and native SiO_2 as the noncatalytic surface. Additionally, we showed that by choosing the right polymer, ASE can be achieved both in oxidative and non-oxidative atmospheres, and over a wide temperature range. Furthermore, we showed that the catalytic effect can be achieved with a very small amount of catalytic material, even less than a monolayer.[2] We demonstrated this with two catalytic materials, Pt and CeO_2. This means that metal surfaces can be converted to catalytic by depositing a small amount of Pt and dielectric surfaces by a small amount of CeO_2.

Here, we show that most metal oxide and nitride surfaces are noncatalytic, or their usage as a catalytic surface is unclear. We demonstrate this by testing two polymers, PMMA and PLA, in three different atmospheres, O_2, H_2, and inert. However, we convert a noncatalytic dielectric surface, HfO_2, to catalytic by depositing 30 cycles of ALD-CeO_2 (< 1 nm). After this, we deposit a line pattern of another noncatalytic material, TiO_2, via direct atomic layer processing (DALP®). We then spin-coat ~40 nm PMMA film on top and pattern the PMMA film by ASE in air. Finally, we deposit 50 cycles of ALD-ZrO_2 (~5 nm) area-selectively, using the ASE-patterned PMMA film as an inhibition layer. Furthermore, we show that only a thin layer of the noncatalytic TiO_2 (~3.5 nm) is enough to deactivate the catalytic effect of CeO_2. Additionally, we show that by increasing the molecular weight of the polymer, we can significantly decrease the polymer flow during the ASE process.

References

1. Zhang et al. Coatings. **2021,** 11, 1124

2. Lasonen et al. Chem. Mater. **2023,** 35, 6097

3. Lasonen et al. Chem. Mater. **2024,** 36, 11645

9:15am **ASD1-TuM-4 Leveraging Topographic Etch Selectivity: Atomic Layer Etch Pitch Splitting (Aps™)***, Robin Athle, Reza Jafari Jam, Yoana Ilarinova, Fabian Veid, Alfred Andersson, Svetlana Ivanova, Kishwar Sultana, Asif Muhammad, Mostafa Torbati, Intu Sharma, Hesamedin Safavi,* AlixLabs A.B., Sweden*; Fred Roozeboom,* University of Twente, Netherlands*; **Dmitry Suyatin**, Jonas Sundqvist, Amin Karimi,* AlixLabs A.B., Sweden

As the semiconductor industry pushes beyond sub-20-nm feature sizes, the limitations of traditional multiple patterning techniques, such as Self-Aligned Double/Quadruple Patterning (SADP/SAQP) and Litho-Etch-Litho-Etch (LELE), become increasingly apparent. These methods rely on complex, multi-step cycles of deposition, lithography, and etching, which escalate costs, increase variability, and significantly increase environmental impact. Atomic Layer Etch Pitch Splitting (APS™) technology enables multiple patterning by utilizing the topographic selectivity of Atomic Layer Etching (ALE) [1-4]. This topographic selectivity transforms nanostructure sidewalls into etch masks, eliminating the need for spacer layer deposition. As a result, APS™ provides a more affordable and sustainable alternative to achieve pitch multiplication with high precision.In this work, we demonstrate the versatility of APS™ across two critical integration paths: high-density scaling by a repeated application of the APS™ process and the APS™ process integration with different lithographic techniques. The process integrates seamlessly into existing industrial workflows, enabling the selective removal of material from the center of pre-patterned features. We show that initial features with critical dimensions (CDs) below 100 nm can be split without additional lithography steps or sacrificial spacer layers, achieving results comparable to state-of-the-art patterning techniques such as immersion ArF lithography (ArFi), Extreme Ultraviolet lithography (EUVL), and Nanoimprint lithography (NIL). At the same time, the reduced process complexity of APS™ directly translates into lower capital expenditures (CAPEX) and operating costs (OPEX), higher throughput, and reduced CO2-equivalent emissions. These advantages position APS™ as a sustainable and scalable solution for next-generation logic and memory devices, offering a pathway to advanced resolution that bypasses the complexity and high costs of traditional multi-patterning.References:1. Khan Md S. A., et al. US10930515 B2, Feb. 23, 2021, priority date March 14, 2017.2. Khan Md S. A., et al. US11424130 B2, Aug. 23, 2022.3. Khan Md S. A., et al., US20250259851 A1, Aug. 14, 2025.4. Sundqvist J., et al. Advanced Etch Technology and Process Integration for Nanopatterning XIV. Vol. 13429, p. 134, SPIE, Apr. 22, 2025.

9:30am **ASD1-TuM-5 Phase and Surface Facet Dependent Etching of High-k Oxides for Selective Atomic Layer Etching***, **Michael Nolan**, Rita Mullins,* Tyndall Institute, Ireland

Thermal Atomic Layer Etching (ALE) is investigated for its potential to deliver atomic level control over the etch of many materials and shows potential for use in future CMOS nodes with requirements for sub-nm levels of control on complex structures. It is performed using sequential surface modification and volatile release reactions. For metal oxides, HF fluorinates the initial surface to form a MF4 layer (M = metal) which undergoes ligand-exchange with precursors such as TiCl4 or SiCl4, which volatilizes the MF4 layer. The question of the role of the phase and surface facets in a deposited high-k metal oxide film has received little attention but can be addressed with first principles atomistic simulations. In this contribution we use density functional theory simulations to explore the effect of the phase and surfaces of HfO2 and ZrO2 on the HF modification half-cycle of ALE. The models used in this study representing polycrystalline materials are the (111) and (001) surface facets of monoclinic, orthorhombic and tetragonal HfO2 and ZrO2. Our thermodynamic analysis shows that for polycrystalline HfO2 and ZrO2, the HF pulse reacts in a self-limiting manner, and is preferred up to processing temperatures that are sensitive to the phase and surface. Models of HF coverage are used to compute calculated theoretical etch rates for the different oxide phases and surface facets and these show a strong dependence on both the crystal phase and the surface so that if different phases and facets are present an uneven etch profile will be seen. The stability, geometry and surface atomic coordination environments drive this dependence.

9:45am **ASD1-TuM-6 Enabling Bottom-up Gap Fill and Selective Metal Deposition via NH3 Plasma-based AS-ALD***, Yoenju Choi, Jeong Hyun Park, Yoona Choi, **Woojin Jeon**,* Kyung Hee University, Republic of Korea

Atomic layer deposition (ALD) has attracted significant attention for next-generation semiconductor manufacturing due to its precise thickness control and excellent step coverage. In addition, active research has been conducted on realizing sub-10-nm devices with extremely high aspect ratios

through area selectivity using small-molecule inhibitors, as well as on the fabrication of vertical structures by controlling chemisorption behavior depending on the substrate.

In this presentation, we introduce the results of area-selective atomic layer deposition (AS-ALD) enabled by plasma treatments. First, we demonstrate an approach to improve gap-fill characteristics by exploiting the inherently poor step coverage of plasma processes. During SiO_2 ALD, NH_3 plasma (NH_3^*) treatment reduces the growth per cycle (GPC) due to inhibited chemisorption of the DIPAS precursor. By incorporating an NH_3^* treatment step into the SiO_2 ALD sequence for patterned structures, SiO_2 deposition is suppressed at the opening region, resulting in bottom-up gap-fill growth behavior.

We also present Co AS-ALD results on TiN and SiO_2 using NH_3^* treatment. The NH_3^* treatment simultaneously induces a decrease in GPC on SiO_2 and an increase in GPC on TiN. This behavior is attributed to suppressed chemisorption of the $CpCo(CO)_2$ Co precursor on SiO_2 due to surface NH_x termination, while on TiN, precursor chemisorption is enhanced by the removal of surface TiO_xN_y species.

These results indicate that NH_3^* treatment is a promising approach for enabling AS-ALD across a wide range of materials and device structures.

10:00am **ASD1-TuM-7 Perfect Selectivity vs Practical Sustainability in ASD***,* ***Nupur Bihari,*** Lam Research Corporation

Area selective deposition (ASD) is increasingly viewed as a critical enabler for advanced semiconductor manufacturing, yet the pursuit of perfect selectivity often introduces excessive process complexity, high precursor consumption and limited sustainability. In this work, we investigate the balance between selectivity and practical process efficiency, with an emphasis on reducing precursor usage while maintaining integration-relevant performance. An eco-friendly process regime is demonstrated to provide robust selectivity without relying on aggressive chemistries or extended exposure conditions. Top-down scanning electron microscopy (TDSEM) is employed as a simple and effective metrology approach to evaluate selectivity, nucleation behavior and pattern fidelity under reduced precursor flow. The results show that excellent selectivity can be achieved with significantly lower precursor usage. Electrical resistance-capacitance (RC) characteristics and integration data indicate that ASD processes with minor selectivity loss still offer compelling advantages for patterning and interconnect scaling. These findings highlight that perfect selectivity is not a prerequisite for successful ASD implementation. Instead, a pragmatic approach that prioritizes precursor efficiency, environmental impact and integration robustness provides a more realistic and sustainable pathway for the adoption of ASD in high volume semiconductor manufacturing.

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