Monday Morning, June 23, 2025

Plenary Session
Room Tamna Hall A - Session PS-MoM

Plenary Session

Moderators: Heeyeop Chae, Sungkyunkwan University (SKKU), **Han-Bo-Ram Lee**, Incheon National University

8:45am **PS-MoM-1 ALD Welcome and Introductory Remarks**,

9:00am **PS-MoM-2 ALD Plenary Lecture: The Evolution of DRAM: Scaling Challenges, ALD Innovations, and Future Architectures**, ***Seiyon Kim***, SK hynix, Republic of Korea **INVITED**

For decades, Dynamic Random Access Memory (DRAM) has been the cornerstone of main memory in computing, meeting the demands of an ever-expanding workload. The need for greater capacity, higher bandwidth, and lower power consumption has continually driven advancements in DRAM technology. The recent surge in artificial intelligence (AI) applications has further accelerated the demand for high-speed memory, catalyzing the rise of High Bandwidth Memory (HBM). While the success of HBM underscores the importance of packaging innovations, traditional scaling continues to play a critical role in improving DRAM core die performance, such as power efficiency, area, and cost, ensuring its competitiveness.

DRAM is primarily composed of three key components: the cell transistor, storage node (SN) capacitor, and peripheral transistor. Each component presents unique scaling challenges due to differences in structure and functionality, yet they share similar material requirements. These include the ability to accommodate nanometer-scale dimensions, achieve high aspect ratios, and meet specific electrical property demands. Atomic Layer Deposition (ALD) has been instrumental in enabling advanced DRAM technology by providing atomically precise control over thickness, composition, and conformality.

As 2D DRAM approaches its scaling limits at sub-10nm nodes, next-generation architectures such as $4F^2$ vertical gate DRAM (VG-DRAM) and lateral 3D DRAM are emerging as potential solutions. VG-DRAM offers significant benefits in scalability and performance, though its implementation has posed considerable challenges. However, recent advancements in process technologies have revitalized its potential as a strong contender for next-generation DRAM. Meanwhile, lateral 3D DRAM presents unique advantages for future extensions by circumventing the limitations of areal scaling.

Future opportunities for ALD materials are vast, particularly in addressing the demands of these new architectures. For example, lateral 3D DRAM relies heavily on lateral processes with exceptional conformality and uniformity across hundreds of layers, which is challenging even for ALD technique. Furthermore, new ALD materials may enable more disruptive capacitor-less DRAM based on 2T gain cells or ferroelectric FET.

This presentation will provide an overview of DRAM applications and key components, highlighting the primary challenges in scaling and the critical role of ALD in overcoming these obstacles. Finally, the discussion will explore the future evolution of DRAM architectures and the new opportunities that lie ahead.

9:45am **PS-MoM-5 ALD 2025 Innovator Awardee Talk: Atomic Layer Deposition of Metal Phosphates and Metal Borates through Thermal and Plasma Activated Approaches**, ***Christophe Detavernier***, Ghent University, Belgium **INVITED**

Metal (boro)phosphate coatings are of interest for a wide range of applications, in particular for lithium ion batteries, electrocatalytic water splitting, and as biocompatible and protective coatings. In view of the need for thickness control and conformality in these applications, there has been a growing interest in developing ALD-based approaches for the deposition of such coatings.

Identifying a suitable phosphate precursor has proven a major challenge. In theory, phosphoric acid would be an ideal candidate, but its use in vapor deposition is prohibited by its low vapor pressure at room temperature and its tendency to decompose rather than evaporate upon heating. Trimethyl phosphate (TMP) is an attractive alternative, offering a vapor pressure of 15 mbar at 70°C. Thermal ALD processes using TMP have been demonstrated for a variety of metal sources, but it has proven difficult to incorporate a sufficiently high atomic percentage of phosphorus in the growing film, requiring an unpractically large number of phosphate sub-cycles for each metal pulse.

Dobbelaere et al. (*Chem. Mater.* 26, 6863 (2014)) explored the use of a TMP plasma, where the TMP precursor vapor is introduced into an inductively coupled plasma (ICP) discharge. At low substrate temperatures, exposure to a TMP plasma results in CVD-type coating in a process akin to plasma polymerisation. However, at sufficiently high substrate temperatures (300°C), saturated growth could be achieved in a true ALD regime, resulting in ALD growth of Al phosphate. Similar TMP-plasma based approaches proved successful for ALD of Ti, V, Zn, Sn, Fe, Ni, Co phosphates, as summarised in the review by Henderick et al. (*J. Appl. Phys. Rev. 9*, 011310 (2022)).

Inspired by the TMP-plasma based approach, Dhara et al. explored plasma activation of trimethyl borate (TMB) towards ALD of Al borate. Using TMB alone in the plasma form does not yield self-limiting ALD growth, as polymerized species continuously accumulate on the substrate. By co-dosing H_2O in the TMB plasma, saturated growth of Al borate films could be achieved at and above 250°C, with a high growth per cycle (~3.5 Å).

10:45am **PS-MoM-9 ALE Welcome and Introductory Remarks**,

11:00am **PS-MoM-10 ALE Plenary Lecture: Challenges and Future of ALE Technology in Semiconductor Manufacturing**, ***Chanmin Lee***, Samsung Electronics, Republic of Korea **INVITED**

Atomic Layer Etching (ALE) has rapidly emerged as a transformative technology in semiconductor manufacturing, enabling atomic-scale precision in material removal that is essential for the fabrication of advanced semiconductor. Conventional etching techniques such as Reactive Ion Etching (RIE) face inherent limitations, including ion-induced damage and aspect ratio-dependent etch (ARDE) effects, which hinder their effectiveness in fabricating high-aspect-ratio and three-dimensional structures. ALE, with its self-limiting, atomic-scale precision, offers a effective alternative by minimizing plasma physical damage and supressing loading effect, even in complex device architectures.

Currently, mass production in the semiconductor industry relies mainly on RIE and Chemical Vapor Deposition (CVD) processes. However, the integration of ALE with Atomic Layer Deposition (ALD) is increasingly being adopted for the fabrication of advanced DRAM, 3D NAND and gate-all-around (GAA) transistors. ALE's selective etching capabilities are proving indispensable for challenging applications such as wafer trench patterning and precise interface engineering in advanced device, achieving levels of precision unattainable by conventional methods.

Despite these advantages, several challenges remain for the widespread adoption of ALE in high-volume manufacturing. These include limited throughput due to the inherently sequential nature of ALE cycles, difficulties in fine-tuning plasma parameters, and the lack of perfect and ideal anisotropic etching with atomic-scale process control. Challenges such as process throughput, scalability, and atomic-level precision will be discussed, along with strategies for overcoming these barriers through synergistic integration with conventional etching and ALE technology.

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