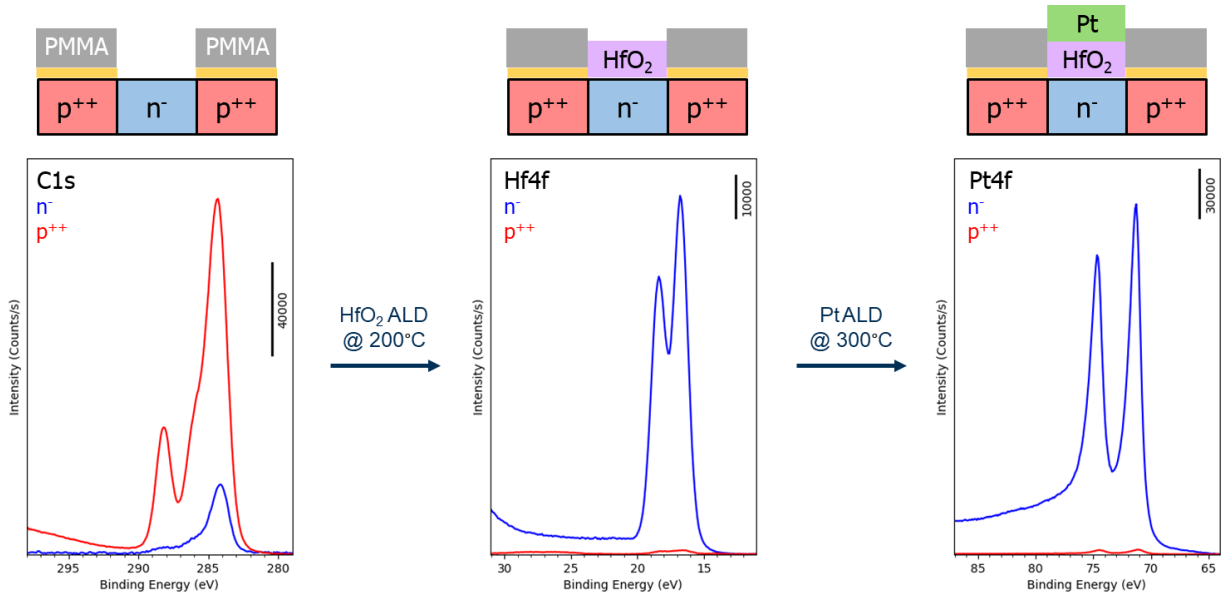
Dopant-Selective Atomic Layer Deposition (DS-ALD) for fabrication of electronic devices

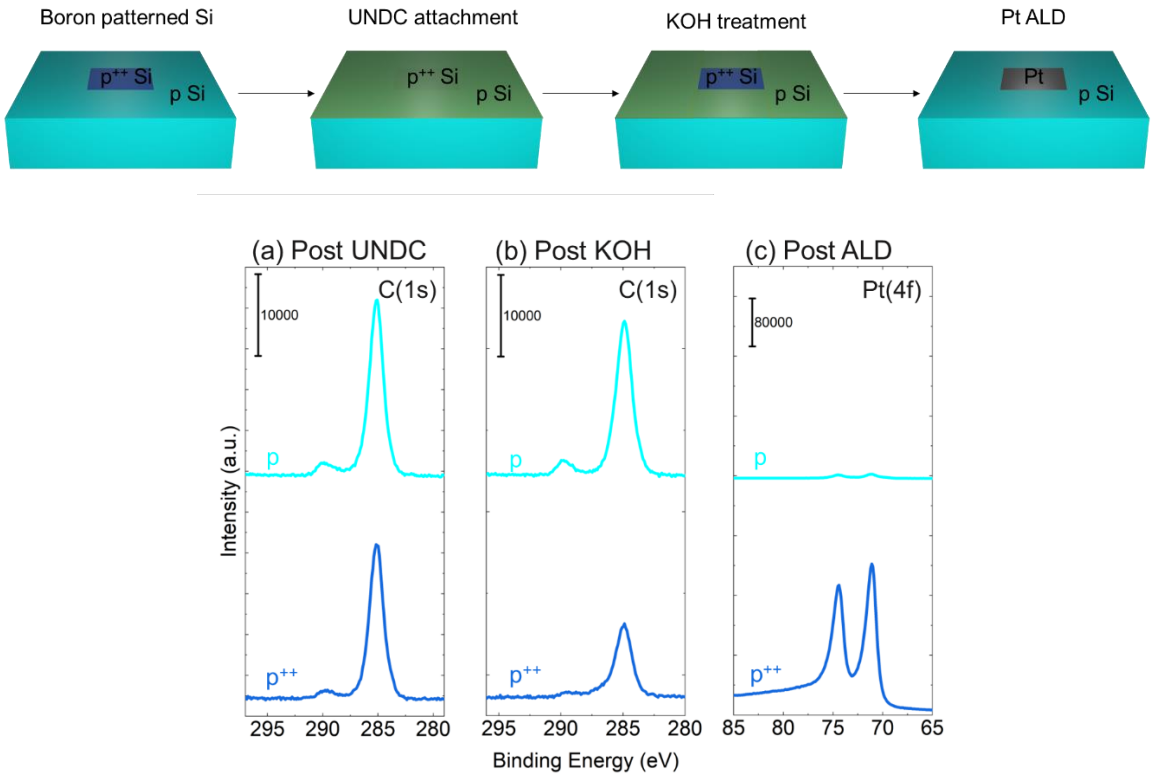
Daniel Aziz[1], Nishant Deshmukh[1], Ryugo Shimamura[2], Amy Brummer[3], Kaifan Yue[5], Siddharth Kurup[3], Kira Barton[6], Eric Vogel[3], Michael A. Filler[1]

[1]Georgia Institute of Technology, College of Engineering, School of Chemical and Biomolecular Engineering, 311 Ferst Dr NW, Atlanta, GA 30332
[2]The University of Tokyo, College of Engineering, Semiconductor Manufacturing Technology, 7 Chome-3-1 Hongo, Bunkyo City, Tokyo 113-8654, Japan
[3]Georgia Institute of Technology, College of Engineering, School of Material Science and Engineering, 771 Ferst Dr NW, Atlanta, GA 30332
[4]Georgia Institute of Technology, College of Engineering, School of Electrical and Computer Engineering, 777 Atlantic Dr NW, Atlanta, GA 30332
[5]University of Michigan at Ann Harbor, College of Engineering, Department of Robotics, 2505 Hayward St, Ann Arbor, MI 48109
[6]University of Michigan at Ann Harbor, College of Engineering, Department of Robotics and Department of Mechanical Engineering, 2505 Hayward St, Ann Arbor, MI 48109

MOSFET gate formation process [1]:



Metal-semiconductor contact formation process [2]:



References:

[1] D. Aziz, et al. Scalable patterning of silicon microstructures for electronics applications. **In preparation** (2025).

[2] N. Deshmukh, D. Aziz, et al. Dopant selective atomic layer deposition of Pt for semiconductor contacting. **In preparation** (2025)