Area Selective ALD
Room Tamna Hall A - Session AS-TuA
Area Selective Deposition I

Moderators: Stacey Bent, Stanford University, **Mikko Ritala**, University of Helsinki

4:00pm **AS-TuA-11 Surface Chemistry Characterization for Area-Selective Atomic Layer Deposition of Ruthenium***, **Eun-Hyoung Cho**,* 2D Device TU(SAIT)/Samsung Electronics, Republic of Korea*; Young Min Lee, Yunseong Lee, Youngchul Leem, Giyoung Jo, Jeong Yub Lee, Kyung-Eun Byun, Jung Yeon Won, Bongsu Kim, Byeong Gyu Chae,* Samsung Advanced Institute of Technology, Republic of Korea*; Kyeongmin Min, Han-Bo-Ram Lee,* Incheon National University, Republic of Korea*; Iaan Cho, Myeong Kyun Nam, Bonggeun Shong,* Hongik University, Republic of Korea **INVITED**

Achieving atomic-scale precise control over material layering is critical for the development of future semiconductor technology. Area-selective deposition (ASD) has emerged as an indispensable tool for crafting semiconductor components and structures via bottom-up pattern transfer. The most widely used approach for ASD relies on self-assembled monolayers (SAMs) to deactivate specific surfaces. However, alternative strategies are being explored to better align with the requirements of high-volume device manufacturing and address the limitations of the SAM method. One promising alternative involves the application of small molecule inhibitors (SMIs). However, limited research has been conducted to elucidate the mechanisms governing their adsorption and inhibition of deposition. Additionally, research on elucidating the ASD mechanism, in which precursors are blocked rather than chemically adsorbed on SMIs, has predominantly relied on simulations such as density functional theory (DFT) calculations or Monte Carlo (MC) simulations. By closely investigating these interfacial phenomena using precise surface analysis techniques, a deeper understanding of the role that SMI composition and structure play in adsorption and inhibition can be achieved, ultimately contributing to the design of SMIs for future ASD systems. Recently, it was confirmed that by controlling the crystal orientation of metal grains, atomic layer deposited ruthenium (Ru) thin films on amorphous dielectric substrates exhibit electrical resistivity comparable to that of single crystal Ru. However, the oxidative counter-reactants such as O2 often used for atomic layer deposition (ALD) of metallic Ru films result in a considerable increase in contact resistance because of substrate oxidation, limiting the applications of both ALD and ASD of Ru. In this study, Ru ASD is demonstrated using two-step ALD with the sequential use of H2 and O2 as counter-reactants and dimethylamino-trimethylsilane (DMATMS) as a precursor inhibitor. Both theoretical and experimental results demonstrate that in the two-step Ru ALD, the oxide layer can be eliminated via the reduction of the oxidized substrate metal surface by the H2 counter-reactant. This mechanism simultaneously facilitates the adsorption of the Ru precursor (tricarbonyl-(trimethylenemethane)-ruthenium) and removal of the surface oxide layer. Consequently, Ru growth is suppressed on the DMATMS-inhibited SiO2 surface during ASD, enabling exclusive deposition of Ru on the Mo surface. The currently proposed Ru ASD scheme using two-step ALD is highly promising for driving advancements in interconnect technology for commercial applications.

4:30pm **AS-TuA-13 Area-Selective Solid-State Synthesis of Nickel Silicide Nanostructures***, **Gabriele Botta**,* Nanogune, Italy*; Mato Knez,* nanogune, Croatia

Over the past decade, metal silicides have been re-discovered for their significant potential across various fields of nanotechnology. [1,2,3] However, integrating them into modern devices continues to pose challenges, primarily due to limited control over phase formation during their synthesis. [4] Additionally, since they are typically grown as continuous layers, their structuring often relies on complex top-down patterning techniques, which significantly limit their practical applications. [5] This study addresses these issues by proposing a method for Area-Selective (AS) silicidation (Fig. 1a SD). Our approach ensures that during material synthesis, the resulting silicide nanostructures acquire a predefined morphology and nucleate exclusively in the targeted regions of the substrate.

The AS silicidation process is demonstrated through the formation of $NiSi_2$ structures on Si(100) and Si(111) substrates (Fig. 1b SD), and its broader applicability is further illustrated with the successful AS synthesis of Cu_3Si (Fig. 1c SD). To direct growth, the silicon substrates are patterned using ion beams, which create surface defects that promote silicide nucleation in the desired areas. Unlike conventional Solid State (SS) synthesis, which involves annealing a metal thin film on silicon, our method begins with an ALD deposited metal oxide. Silicidation is performed by annealing in the presence of a reductant (H_2), which reduces the metal oxide to its metallic state. The resulting metal then reacts with the underlying silicon, forming a metal silicide. During this two-step reaction, the material re-arranges along surface defects, which act as templates, guiding both the shape and positioning of the forming silicide crystals.

The effectiveness of this multi-step fabrication method, coupled with its adaptability to various metal-silicide systems, underscores its potential to create functional, structured silicides without the need for post-synthesis nanopatterning.

References

1. Z. He, Y. He, Y. Qiu, Q. Zhao, Z. Wang, X. Kang, L. Yu, L. Wu, Y. Jiang, Appl. Catal. B Environ. 2024, 342, 123386.
2. Y. Niu, K. Zhang, X. Cui, X. Wu, J. Yang, Nano Lett. 2023, 23, 2332–2338.
3. R. Reichlova, H. Lopes Seeger, R. González-Hernández, Nat. Commun. 2024, 15, 4961.
4. Y. C. Chou, L. J. Chen, K. N. Tu, Nano Lett. 2022, 22, 6895–6899.
5. N. Breil, C. Lavoie, A. Ozcan, F. Baumann, N. Klymko, K. Nummy, B. Sun, J. Jordan-Sweet, J. Yu, F. Zhu, S. Narasimha, M. Chudzik, Microelectron. Eng. 2015, 137, 79–87.

4:45pm **AS-TuA-14 ALD Outstanding Presentation Award Finalist: High Temperature Area Selective ALD SiN by in-Situ Selective Surface Fluorination***, **Haonan Liu**, Ken Okoshi, Hiroki Murakami, Yamato Tonegawa,* Tokyo Electron Technology Solutions Ltd., Japan

Presently, research on area selective atomic layer deposition (AS-ALD) is attracting strong interest. AS-ALD simplifies the process of deposition on patterned substrates and high aspect ratio (AR>70) structures, holding promise for various applications in semiconductor manufacturing. Inhibitors such as self-assembled monolayers (SAMs) and (dimethylamino)trimethylsilane (DMA-TMS) are typically used to passivate non-growth areas.[1] However, the deterioration of selectivity at temperatures exceeding 500℃ limits their applications in high temperature deposition processes. Fluorination is regarded as a candidate for overcoming these problems.[2] In this study, we present a novel approach to achieve high selectivity in high temperature AS-ALD on SiN versus SiO_2 through effective surface-selective fluorination without damage to the substrates.

Experiments were conducted with a batch furnace capable of treating over one hundred 300 mm wafers simultaneously. A wide range of substrates were utilized including 300mm wafers with blanket SiN and SiO_2 films and various nanostructured samples. Prior to inhibition, samples were precleaned by dilute HF to remove native oxides. An HF gas passivation was employed at 630℃ for 10 minutes to selectively inhibit the SiO_2 surface. ALD SiN was deposited with dichlorosilane (SiH_2Cl_2) as the precursor and NH_3 as the co-reactant at 630 ℃.

The initial AS-ALD sequence involved performing ALD cycles following HF passivation, resulting in AS-ALD of up to 6 nm SiN on SiN while maintaining good within-wafer non-uniformity (Win Unif.) of <3%. We then developed the area-selective-deposition-Loop (ASD-Loop) technique, consisting of alternating 10-minute HF passivation with ALD cycles, as shown in Figure 1. We achieved an AS-ALD of 28 nm on SiN blanket wafers with high selectivity while keeping excellent Win Unif. of <2% and high film quality, as confirmed by the wet etching rate. The ASD-Loop has also been successfully applied to SiN/SiO stripe-patterned substrates (Figure 2), resulting in a maximum ASD thickness of 21 nm; and to high-AR holes on SiO_2/SiN stacks (Figure 3), resulting in AS-ALD with high conformality of >90%. Thus, we have demonstrated high-temperature AS-ALD on 300 mm wafers and complex nanostructures with high selectivity, superior uniformity, and reliable quality. This offers a new pathway for the integration of AS-ALD into nanofabrication schemes, showing significant potential for advancing high-performance semiconductor applications including DRAM and 3D NAND manufacturing.

References

1. R. Khan et al., *Chem. Mater.* **2018**, 30, 7603.

2. H. Oh et al., *Adv. Funct. Mater.* **2024**, 34, 2316872.

5:00pm **AS-TuA-15 Mutifunctional Ru/ZnO Bilayer for Sustainable Cu Interconnects using Area-Selective Atomic Layer Deposition of barrier with Small Molecule Inhibitor***, **Minwoo Kim**, Yeseul Son, Sang Bok Kim, Soo-Hyun Kim,* Ulsan National Institute of Science and Technology (UNIST), Republic of Korea

With the scaling of semiconductor devices, the increase in via resistance, which constitutes a significant portion of the Cu interconnect resistance, has emerged as a critical issue. To reduce via resistance, studies [1, 2] have been conducted on forming bottomless barriers using area selective deposition (ASD), where a high-resistivity barrier layer is selectively deposited only on the via/trench sidewalls, SiO_2-based dielectrics without being deposited on the via bottom, Cu. In these studies, self-assembled monolayers (SAMs) with long alkyl chains were used as inhibitors for preventing the adsorption of the precursor on metallic surfaces. However, SAMs are typically adsorbed onto surfaces through solution-based processes, which pose compatibility issues with semiconductor processes and, due to their relatively long molecular structure, cannot form a uniform inhibitor layer within 3D nanostructures. To prevent these issues, this study used a small molecule inhibitor (SMI) to form a bottomless barrier. Additionally, based on previously reported studies [1], the Ru/ZnO bilayer, with ZnO for the bottomless barrier and Ru for the liner and seed layer, was applied for the sustainable Cu interconnects [Figure 1]. The ZnO ASD process is carried out using an amine-based SMI that selectively absorbs on Cu, with diethylzinc and H_2O used for the ZnO ALD process. After the ZnO ASD process and the removal of the inhibitor, the Ru film was deposited using an ALD process with tricarbonyl(trimethylenemethane)ruthenium and O_2. By controlling the conditions of the ZnO ASD process, we confirmed and analyzed the selective deposition of ZnO on the SiO_2-based dielectric substrate not on Cu one using TEM, XPS, and XRD etc. The detailed results will be presented in the conference.

References

[1]Mori, Yuki, et al. Small 19.34 (2023): 2300290.
[2]You, Shi, et al. "Selective Barrier for Cu Interconnect Extension in 3nm Node and Beyond", IITC (2018)

Acknowledgements

This work was supported by the Technology Innovation Program (Public-private joint investment semiconductor R&D program (K-CHIPS) to foster high-quality human resources) (RS-2023-00236667, High-performance Ru-TiN interconnects via high-temperature atomic layer deposition (ALD) and development on new interconnect materials based on ALD) funded by the Ministry of Trade, Industry & Energy (MOTIE, Korea) (1415187401). This work was also supported by SK hynix semiconductor through the cluster research between UNIST and SK hynix semiconductor.

Author Index

Bold page numbers indicate presenter