Atomic Layer Etching
Room Samda Hall AB - Session ALE-MoA

ALD+ALE - Emerging ALE

Moderators: Silvia Armini, IMEC Belgium, **Huichan Seo**, SK Hynix

4:00pm **ALE-MoA-11 Revolutionizing Semiconductor Scaling with Atomic Layer Etch Pitch Splitting**, ***Jonas Sundqvist***, *Reza Jam, Robin Athle, Yoana Ilarionova, Asif Hassan, Intu Sharma, Amin Karimi,* AlixLabs, Sweden*; Fred Roozeboom,* AlixLabs, Netherlands*; Dmitry Suyatin,* AlixLabs, Sweden **INVITED**

We introduce Atomic Layer Etching Pitch Splitting (APS™), a new cost-effective patterning alternative to Self-Aligned Multi Patterning (SAMP) for realizing sub-20-nm features. APS combines atomic-level processes like Atomic Layer Etching (ALE) with existing production techniques, enabling selective etching without the need for the multiple deposition and etch steps required in SAMP. This results in exceptional precision and patterning accuracy, which is crucial for defining critical device features.

The feasibility of APS on silicon and gallium phosphide (GaP) nanowires was previously reported.[1,2] In this study, we apply APS to electron beam lithography (EBL) patterned lines on 300-mm silicon wafers. We achieve a half-pitch of 20 nm and critical dimensions (CDs) below 15 nm on both single-crystalline and amorphous silicon (a-Si) wafers, see Fig. 1. Additionally, when applied to GaP wafers, APS achieves CDs as small as 3 nm (Fig. 2). The layers created by APS can serve as universal split masks for further etching into various materials, including dielectrics, metals, and high-k dielectrics. Alternatively, these structures can be directly used to define critical features such as fins for FinFETs. In addition to the pitch, it is possible to control the CD and height of the fins. The APS process is selective towards different materials, making it a suitable for multi-stack device processing. The gentle nature of APS process minimizes damage to underlying materials, as shown by high-resolution transmission electron microscopy images, Fig. 2.

Unlike its counterparts, APS is free from pattern shrinkage, "bird's beak," tilting, and kinking,[3] and etch damage.[4] This makes APS a highly repeatable process with the potential for high yield and exceptional resolution, which is vital for future semiconductor technology. We estimate that APS may reduce wafer manufacturing costs and increasing throughput. This positions APS as a competitive and complementary alternative to established techniques like SAMP and multiple lithography-etch processes. Furthermore, using less process gases and eliminating several fabrication steps, APS meets industry goals for reduced resource consumption and CO_2 emissions.

References:

1. US Patent 10,930,515, Feb. 23, 2021.

2. US Patent 11,424,130, Aug. 23, 2022.

3. Farrell et al., SPIE, 2018, doi: 10.1117/12.2303004

4. J. Sundqvist et al., SPIE 2025, paper 13429-28.

4:30pm **ALE-MoA-13 Exploring Atomic Layer Etching Behavior Differences in ZnO Crystallographic Planes and Surface Energy Analysis via DFT**, *Jin Seong Park,* ***Ji Hyun Gwoen***, *Hae Lin Yang, Min Chan Kim, Gyeong Min Jeong,* Hanyang University, Korea*; Cas Visser, Erwin Kessels,* Eindhoven University of Technology, The Netherlands

Oxide semiconductor thin films are widely studied for their high electron mobility, uniformity over large areas, and potential for low-temperature processing. These films can be deposited using various methods, including pulsed laser deposition (PLD), molecular beam epitaxy (MBE), chemical vapor deposition (CVD), and sputtering. However, as semiconductor scaling becomes more demanding, precise thickness control and high film quality are increasingly required. To address this, atomic layer processes (ALP), including atomic layer deposition (ALD) and atomic layer etching (ALE), have gained significant attention for their atomic-level precision.

While ALD research on oxide semiconductors has been active since the early 2000s, ALE studies have only gained momentum in the late 2010s and remain relatively limited. Most ALE research has focused on process development and reaction mechanisms, with less emphasis on the characteristics of ALE-processed films, an important aspect for advancing semiconductor technology. Further exploration of ALP, particularly ALE, is crucial for achieving ultra-high integration in semiconductor devices.

In this study, we analyzed the physical properties of ZnO thin films grown by ALD and those processed with both ALD and ALE (ALD+ALE), focusing on crystallinity. The etching behavior of ZnO during ALE was examined experimentally and further analyzed using density functional theory (DFT) simulations. X-ray diffraction (XRD) analysis revealed that the metastable (103) plane appears at a lower thickness in ALD+ALE ZnO films compared to ALD-only films. A significant reduction in the intensity of the (002) plane in ALD+ALE films indicated its preferential etching during ALE. DFT simulations supported this finding by calculating surface energy and adsorption energies of etching reactants. The etch per cycle (EPC) was determined as 0.68 Å/cycle for the (002) plane and 0.53 Å/cycle for the (103) plane, further confirming the preferential etching of the (002) plane.

By integrating DFT simulations with experimental results, we provide a predictive approach to understanding etching behavior. This methodology can be extended beyond ZnO to analyze ALE behavior in other oxide semiconductors, offering valuable insights for future semiconductor processing advancements.

4:45pm **ALE-MoA-14 Investigation of Plasma ALD and ALE of Al_2O_3 in Nanoscale Structures: Towards Corner Lithography at the sub-20 nm Scale**, ***Nicholas J. Chittock***, Oxford Instruments Plasma Technology, UK*; Erwin Berenschot, Niels Tas, Melissa J. Goodwin,* University of Twente, Netherlands*; Marcel A. Verheijen,* Eurofins Materials Science, Netherlands*; Meghali Chopra, Yang Ban,* Sandbox Semiconductor*; Erwin Kessels, Adriaan J.M. Mackus,* Eindhoven University of Technology, Netherlands

Alternative techniques to photolithography are required to facilitate fabrication of 3D nanoscale structures. Corner lithography (CL) is a technique for patterning 3D structures at the wafer scale, that avoids the use of multiple photolithography steps but is limited to features > 20 nm.[1,2] CL is achieved by performing deposition followed by etching, which selectively deposits material only in concave corners. ALD and ALE are perhaps ideal candidates for sub-20 nm CL due to their precise thickness control combined with conformal and uniform deposition and etching, respectively.

In this work, plasma ALD and plasma isotropic ALE of Al_2O_3 are employed on a 3D structure to demonstrate CL at the sub-20 nm scale. Studying the conformal deposition and etching around corners in nanoscale 3D structures provides insight into growth and etch behaviour in these geometries, which can be useful for many different applications (e.g. GaaFET, DRAM, nanoparticle coating). To confirm the isotropic nature of the plasma processes, a 2 nm Al_2O_3 film is deposited on the 3D structure by combining 5 nm of ALD and 3 nm of ALE. Analysis of TEM images post ALD and ALE show that the planar regions of the structure are coated in 2 nm of Al_2O_3. In contrast, a thicker film is observed in the corners compared to the planar regions. By exploiting the enhanced deposition in the corner from ALD, CL is demonstrated by performing 5 nm of ALD and 5 nm of ALE. Post ALD and ALE TEM analysis shows that a ~5 nm thick film is deposited only in the concave corners. The successful demonstration of CL by combining ALD and ALE highlights their utility for fabricating 3D structures at the nm-scale without the use of multiple photolithography steps. In future work, the Al_2O_3 in the corner could then be used as a structural part of a device, or as a mask for further CL processing.[1,2]

1. Jonker, D., *et al,*. (2024). *Electrochemical Sensing with Spatially Patterned Pt Octahedra Electrodes*. Advanced Materials Technologies, 9(5).
2. Ni, S., *et al,*. (2020). Wafer-scale 3D shaping of high aspect ratio structures by multistep plasma etching and corner lithography. Microsystems & Nanoengineering, 6(1), 25.

5:00pm **ALE-MoA-15 Optimizing EUV Etching with In-Situ Atomic Processing: Where and Why?**, ***Philippe Bezard***, IMEC Belgium*; Atefeh Fathzadeh,* KU Leuven and Imec, Belgium

As pattern dimensions shrink with each new manufacturing node, the thickness of many sacrificial patterning stack layers also decreases. This reduction benefits atomic processing by shortening processing time, a key concern in Atomic Layer Etching (ALE). However, a critical question arises: which process steps should adopt atomic processing first, and which should avoid it?

Additionally, the latest etch chambers now offer in-situ PEALD capabilities, enabling fully in-situ spacer-assisted patterning.

This paper explores how atomic processing techniques—such as PE-ALE, PE-ALD, and Transient Assisted Processing (TAP)—can extend the capabilities of conventional etching (RIE) in EUV lithography era. Using a 14 nm pitch Self-Aligned Double Patterning flow as a case study, we

demonstrate how TAP and in-situ PEALD enable simplifications. We then compare ALE, TAP, and RIE across key steps (descum, core etching, spacer deposition, core pull) in terms of roughness, processing time, sustainability (gas and energy consumption), and fundamental limitations. While ALE and TAP significantly outperformed RIE in descum and core etching, evaluating their impact on sustainability and throughput revealed complex and interesting trade-offs due to unique process flow simplifications enabled by these techniques.

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