Atomic Layer Etching
Room Samda Hall AB - Session ALE2-TuM

ALE Applications I

Moderators: Eric A. Joseph, IBM Research Division, T.J. Watson Research Center, **Jonas Sundqvist**, BALD Engineering AB

10:45am **ALE2-TuM-12 Enhancing 3D NAND Flash Memory Production: Addressing High Aspect Ratio Etching Challenges with Atomic Layer Etching**, ***Jaewon Lee***, *Huichan Seo,* SK hynix Inc., Republic of Korea **INVITED**

The fabrication of 3D NAND flash memory presents significant challenges in the etching process, particularly as device architectures scale to higher layer counts. Key issues include achieving precise etch profiles in high aspect ratio (HAR) structures, maintaining uniformity across large wafer areas, and ensuring high selectivity between different materials. Atomic Layer Etching (ALE) has emerged as a promising technique to address these challenges by enabling atomic-scale precision in material removal. However, traditional ALE processes are often limited by slow etch rates, which can impede throughput in high-volume manufacturing. Recent advancements in plasma-enhanced ALE have demonstrated potential in increasing etch rates while preserving the inherent precision of the technique. This abstract discusses the current challenges in 3D NAND etching and explores the development of ALE processes, focusing on enhancing etch rates, improving profile control, and ensuring uniformity across wafers. By advancing ALE technology, it is possible to meet the stringent requirements of next-generation 3D NAND fabrication.

11:15am **ALE2-TuM-14 Controlled Electron-Enhanced Silicon Etching with H_2 Background Gas and Positive Sample Voltage**, *Sumaira Yasmeen,* University of Colorado at Boulder*; Harsono Simka,* Samsung Semiconductor*;* ***Steven George****,* University of Colorado at Boulder

Controlled electron-enhanced silicon etching can be achieved with H_2 background gas and positive sample voltage. Electrons impinged on the silicon surface at normal incidence at currents of ≥200 mA over surface areas of ~4 cm^2. The electron energy was ~140-240 eV defined by the grid bias on the hollow cathode plasma electron source and positive sample voltages. The H_2 pressures were <3 mTorr. The silicon etching for Si(100) and a-Si at room temperature was measured using in situ spectroscopic ellipsometry. The etched silicon thickness was linear versus time during electron-enhanced etching. The etch rates increased progressively with larger positive sample voltages (Figure 1). Si(100) etched slower than a-Si. For example, the etch rates were ~2.6 Å/min for crystalline Si(100) and 9.9 Å/min for a-Si under the same conditions at an incident electron energy of 140 eV with a positive sample voltage of +90 V.

Without the positive sample voltage, the silicon etch rates were negligible. In addition, electron-enhanced Si etching was not accomplished using a D_2 background gas instead of a H_2 background gas. These results support the proposed mechanism for electron-enhanced Si etching where H_2 produces H^- via dissociative electron attachment (DEA) according to $H_2 + e^- \rightarrow H_2^- \rightarrow H + H^-$. The positive voltage on the sample stage then pulls the H^- negative ions to the silicon sample to react with silicon to produce SiH_4 as an etch product (Figure 2). The low energy electrons required for DEA are secondary electrons produced by the primary electrons impinging on the silicon surface.

The energy of secondary electrons from silicon peaks at ~2-3 eV and drops off rapidly at higher energies approaching 10 eV. The peak of the DEA cross section for H_2 is 3.75 eV. In comparison, the peak of the DEA cross section for D_2 is 14.0 eV. The D_2 background gas may not be effective for silicon etching because D^- is not produced by DEA because the secondary electron energy from silicon is too low. These results demonstrate a new mechanism for controlled electron-enhanced silicon etching based on H_2 DEA from secondary electrons and H^- attraction to the positive sample voltage on the silicon sample.

11:30am **ALE2-TuM-15 Suppressing Surface Roughness in Tungsten Wet Atomic Layer Etching using Halogenation**, ***Tulashi Dahal***, *Kate Abel,* Tokyo Electron America Inc.,*; Karthik Pillai,* TEL Technology Center, America, LLC*; Trace Hurd, Antonio Rotondaro,* Tokyo Electron America Inc.,

As the interconnect schemes of leading-edge devices become increasingly complex, there is continued pressure to minimize the via resistance. One path is to minimize post-etch tungsten (W) surface roughness by replacing the current W etch processes with a less damaging approach. Wet Atomic Layer Etching (ALE) offers materials removal in atomic scale in two sequential, self-limiting steps at or near room temperature under ambient pressure without roughening the post-etch morphology. Here we present and compare our results on wet ALE of metallic tungsten (W) using either an oxidizer or a halogenating agent as surface modifying species.

Tungsten surface modification was studied using either an oxidizer or a halogenating agent in appropriate solvents. We expect the hydrolysis of tungsten halides based on their water reactivity so the halogenated surface will be only a reactive intermediate with the passivation layer ultimately composed of hydrolysis product. Solubilization of surface product can be suppressed and self-limiting surface modification of W can be achieved in non-aqueous solutions of oxidizer and halogenating species. Cyclic etch experiments were carried out to estimate the W etch amount per cycle by exposing W coupon in both oxidizing and halogenating solution followed by a rinse step and selective removal of modified layer in second chemistry different than the solvent used in the first step. W ER of ~0.33 nm/cycle (Fig. 1) in halogenating solution is about 2.5 times higher than W ER of ~0.13 nm/cycle achieved from oxidizing solution which may be attributed to the formation of thicker metal halide as surface passivation. The measured RMS roughness (Fig. 2) and the SEM images (Fig. 3) show that surface smoothness [RMS roughness of post-etch coupon ~ (1.109±0.081) nm is lower than as the RMS roughness ~ (1.275±0.130) nm of as deposited W coupon] is improved in post-etch halogenated W coupon up to about 8 nm. We attribute the improved morphology in halogenated post-etch W coupon to the formation of conformal metal halide as surface passivation. The evolution of surface roughness in post-etch W following oxidation route suggest that self-limiting surface modification is the necessary but not the sufficient condition to preserve or improve the surface morphology.

11:45am **ALE2-TuM-16 Plasma-Enhanced Isotropic Atomic Layer Etching of Molybdenum with Fluorocarbon Layer Formation Followed by Plasma Oxidation**, ***Heeju Ha***, *Hyeongwu Lee, Heeyeop Chae,* Sungkyunkwan University (SKKU), Republic of Korea

In this work, plasma-enhanced atomic layer etching (ALE) processes were characterized for molybdenum (Mo) with fluorocarbon deposition in the modification step and oxidation in the removal step. The Mo surface was fluorinated with C_4F_8 or CHF_3 plasma and C_4F_8 shows higher fluorine-contents at the same fluorocarbon layer thickness of 1 nm. The deposition rate of fluorocarbon layer on the Mo surface decreased with increasing temperature and C_4F_8 plasma shows a higher fluorocarbon deposition rate than CHF_3 plasma. The fluorinated surface was removed by oxidation reaction with O_2 plasma. The etch per cycle (EPC) of Mo was observed 0.96 ~ 16 nm/cycle for C_4F_8 plasma and 0.43 ~ 11.2 nm/cycle for CHF_3 plasma in the temperature range of 25 ~ 200 ℃ possibly due to higher fluorine concentration in the fluorocarbon layers. The activation energy for Mo etching obtained from the slope of the Arrhenius plot is 0.18 eV for C_4F_8 plasma and 0.22 eV for CHF_3 plasma. Fluorine residue after ALE was as low as 6%, which is attributed to the Mo_2CF_x peak.

Author Index

Bold page numbers indicate presenter