

Supplemental Document:

Atomic Layer Deposition of Interface-Engineered $\text{Li}_4\text{Ti}_5\text{O}_{12}$: Toward High-Capacity 3D Thin-Film Batteries

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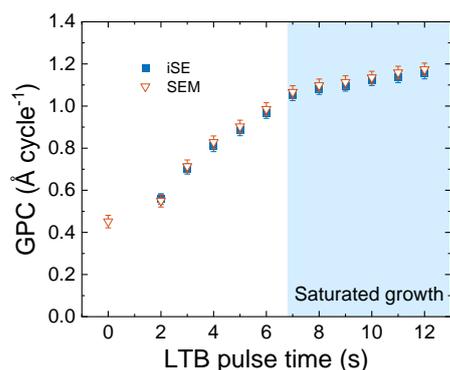


Figure 1: LTB pulse time-dependent GPC for an ALD process fabricating $\text{Li}_4\text{Ti}_5\text{O}_{12}$ thin films.

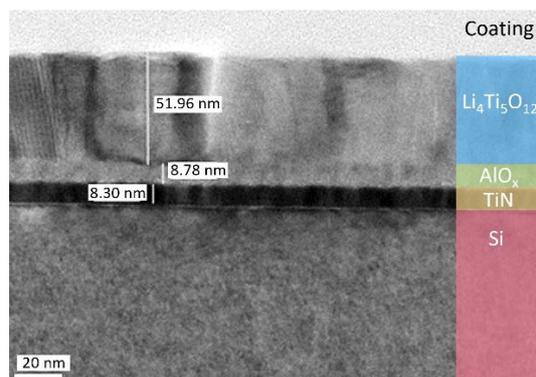


Figure 2: TEM micrograph of the battery layer stack with a 100-cycle AlO_x interlayer.

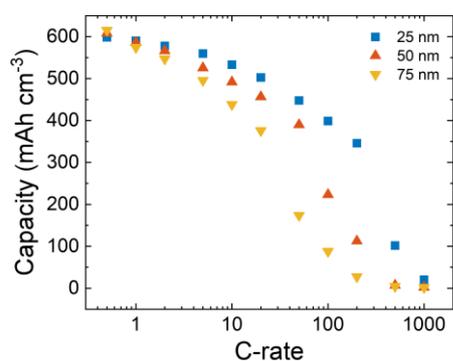


Figure 3: C-rate performance of ALD LTO thin films with different thicknesses.

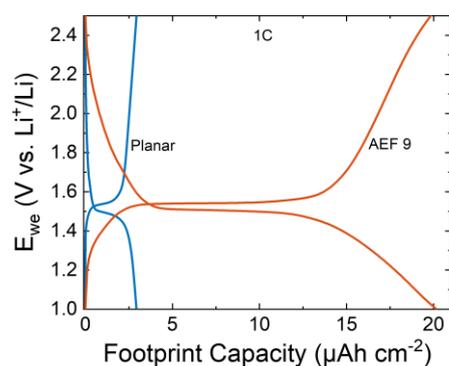


Figure 4: Footprint capacity for planar and 3D LTO films with a thickness of 50 nm.

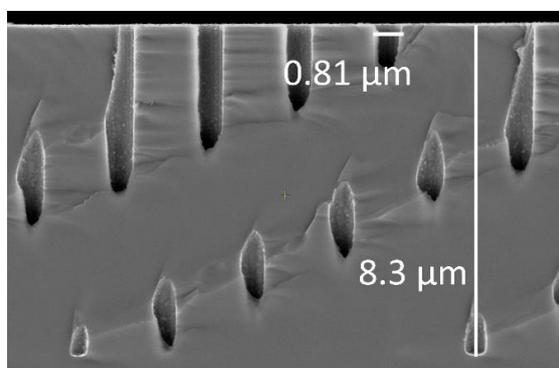


Figure 5: Cross-section SEM micrograph of the structured Si substrate for conformality tests.

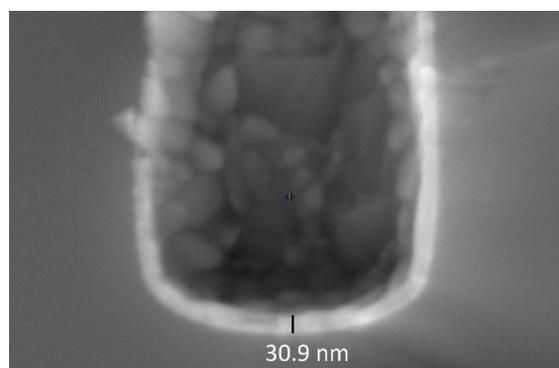


Figure 6: Cross-section SEM micrograph of the bottom of a hole with a 10:1 aspect ratio.