Supplemental Document

Figure 1a illustrates the schematics of the ALD-IGZO Top-gate TFT structure with gate insulator of Al_2O_3 (A20), SiO_2 (S20), and SiO_2/Al_2O_3 (SA). Figure 1b shows the electrical properties of single and heterogeneous gate insulator TFTs. Figure 1c is the representative transfer curves for A20, S20, and SA-TFTs under PBTS conditions (electric field = 2 MV/cm and temperature = 60 ℃ for 1 h). Figure 1d is the constant current stability (CCS) of A20-, S20, and SA-TFTs under V_{GS} = 4 V and V_{DS} = 1 V for 1 hour with the illustration of the reliability compensation concept based on the quantitative comparison between electron trapping sites in gate insulator and donor-induced species in A20-, S20-, and SA-TFTs.

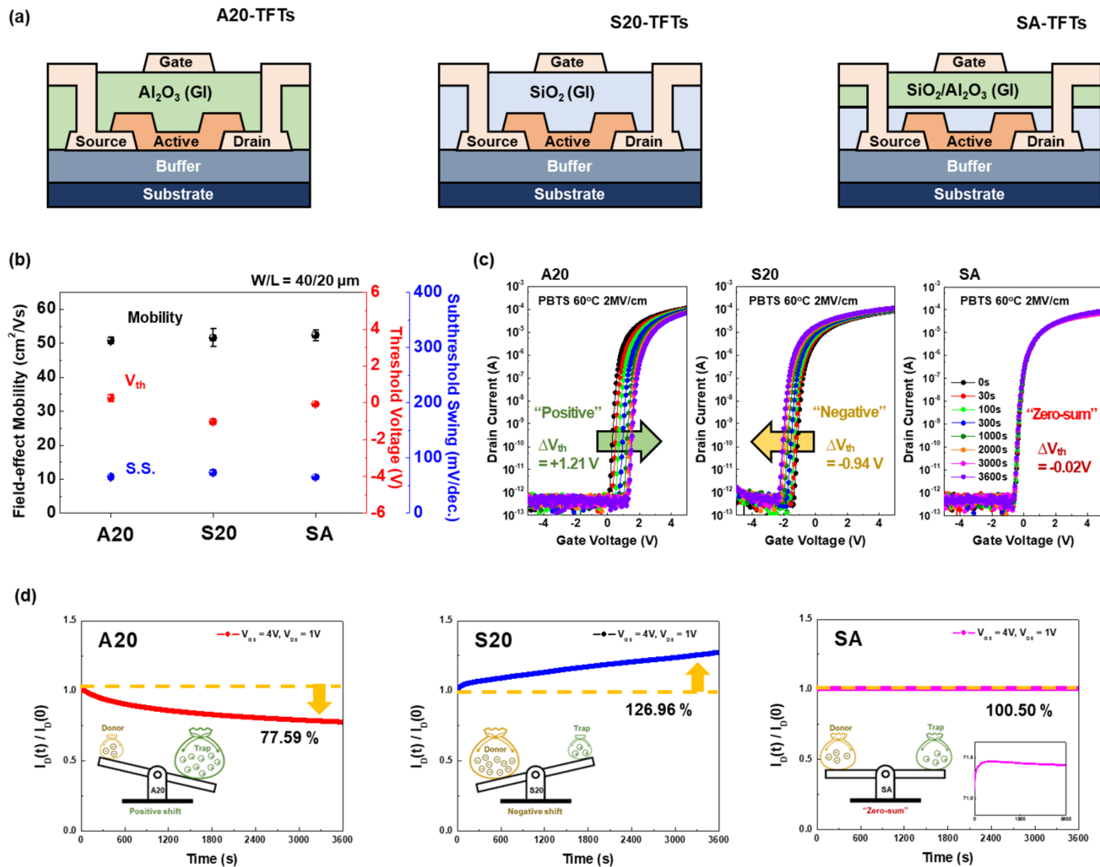

Figure 1. (a) Schematics of ALD-IGZO Top-gate TFT structure with gate insulator of Al_2O_3 (A20), SiO_2 (S20), and SiO_2/Al_2O_3 (SA). (b) Summary of electrical properties of single and heterogeneous gate insulator TFTs (average value (± standard deviation) extracted from evaluated devices. (c) Representative transfer curves for A20, S20 and SA-TFTs under PBTS condition (electric field = 2 MV/cm and temperature = 60 ℃ for 1 h). (d) The constant current stability (CCS) of A20-, S20, and SA-TFTs under V_{GS} = 4 V and V_{DS} = 1 V for 1 hour with the illustration of the reliability compensation concept based on the quantitative comparison between electron trapping sites in gate insulator and donor-induced species.