Supplemental Document

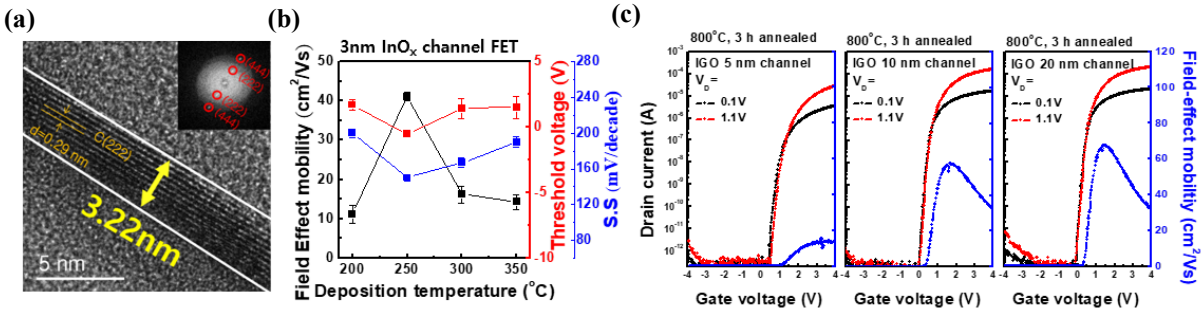

Fig. 1 (a) HRTEM and (b) electrical properties summary of InO films and channel FET deposited ALD method using DBADMIn precursor [2]. The transfer and field-effect mobility of gallium doped InO (IGO) channel FET after the 800 ºC post-annealing process for 3 hours according to the thickness.

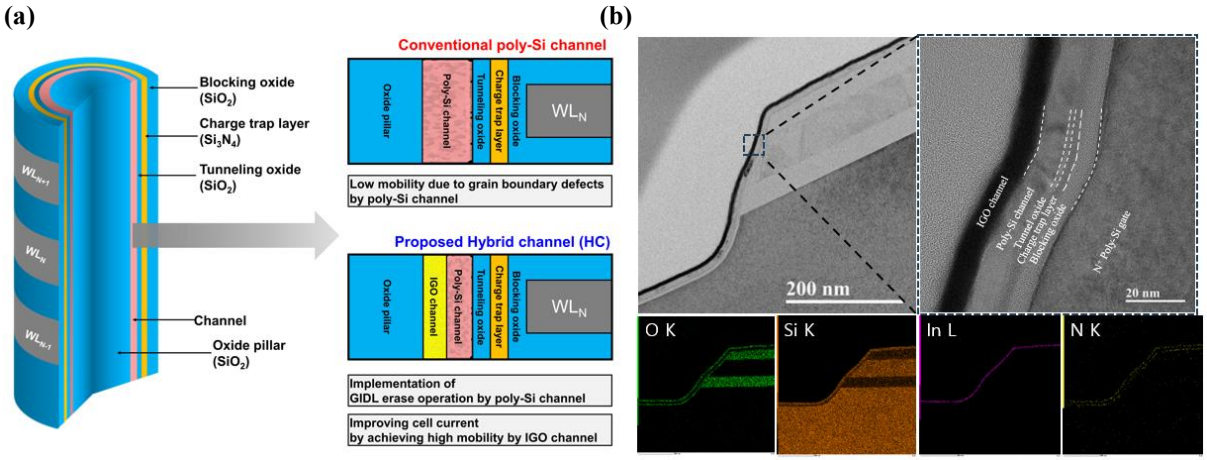

Fig. 2 (a) Schematic of 3D NAND flash memory structure for illustrating of conventional poly-Si and purpose of hybrid-channel (HC) structure. (b) Cross-sectional HRTEM image and EDAX results of the fabricated vertical structure charge trap NAND Flash memory device.

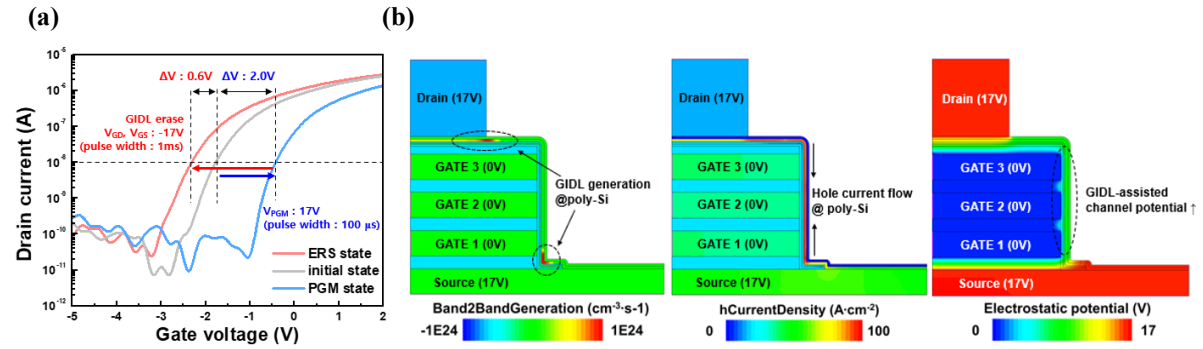

Fig. 3 (a) measured I-V curve of initial, program, and erased state of fabricated vertical channel structure charge trap NAND Flash memory device. And TCAD simulation for illustrating GIDL erase mechanism (b) band-to-band generation, (c) hole current density, (d) electrostatic potential of 3-layer stacked structure.