Investigation of Thermal Atomic Layer Deposition for Vertical-Channel IGZO FET with Good Performance and Thermal Stability

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Emerging computing applications such as ChatGPT and AR/VR are demanding memory chip for larger capacity and lower power consumption. IGZO-based DRAM has attracted considerable attention recently due to the extremely low off-current and BEOL compatibility of IGZO FETs. And vertical channel transistors are a promising approach to realizing 3D DRAM. In this work, we utilized thermal ALD process to deposit IGZO channel for vertical channel FET. By utilizing a fully thermal ALD process during IGZO-channel/GI deposition and applying appropriate gate film stack, the fabricated vertical channel FET exhibits good device performance and thermal stability, which is an excellent result among ALD-IGZO FETs.

The cross-sectional view and top-down view of a vertical channel IGZO FET are shown in Fig.1(a) and (b), respectively. The top and bottom source/drain electrode layers are vertically separated by a spacer layer. The channel area is located on the sidewalls of S/D-spacer-S/D stack layers and the channel length (L) is defined as the thickness of the spacer layer. According to the top view (Fig. 1(b)), the S/D-spacer-S/D sidewalls form a circle. Therefore, the channel width (W) is defined as the circumference of this circle. Fig. 1(c) shows the fabrication flow of a vertical channel IGZO FET. After patterning the bottom TiN S/D layer, a SiO spacer layer and a top TiN S/D layer are sequentially deposited. The top S/D and spacer layers are sequentially patterned for pad formation and pad open. To form the channel hole region, the S/D-spacer-S/D stack is sequentially etched. Vertical channel FET requires excellent trench coverage and film uniformity of the channel film, so ALD is an ideal channel-GI deposition process, and O_3 is selected as the oxidant for the ALD process. The IGZO film and HfO film are sequentially deposited through this thermal ALD process to form a channel-GI film stack. After that, IZO-TiN-W is deposited sequentially as a gate film stack. The gate stack is finally patterned for the device isolation and a vertical channel IGZO FET is obtained.

Fig. 2 shows the transfer and output characteristics of the fabricated vertical channel IGZO FETs. According to the transfer curve, the IGZO FETs show good performance with a large on-off ratio. To evaluate the thermal stability of the fabricated IGZO FETs, the devices were annealed at 350°C, and the post-annealed transfer and output characteristics are shown in Fig. 3. Fig. 3 shows that the annealed IGZO FETs still maintains the good characteristics with improved contact behavior, indicating that the fabricated IGZO FETs have reasonably good thermal stability. To better compare the device performance before and after annealing, Fig. 4 shows the statistical results of the extracted device parameters before and after annealing, the degraded SS after annealing may need further optimization. The above results provide a reference for the implementation of high-performance IGZO FETs.

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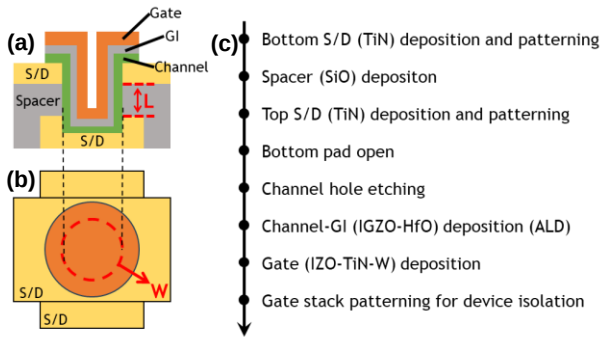

Figure 1. (a) Cross-sectional and (b) Top-down views of a vertical-channel IGZO FET. Channel length (L) is defined as the thickness of the spacer layer, and channel width (W) is defined as the circumference of the circular sidewall. (c) Fabrication flow of a vertical-channel IGZO FET.

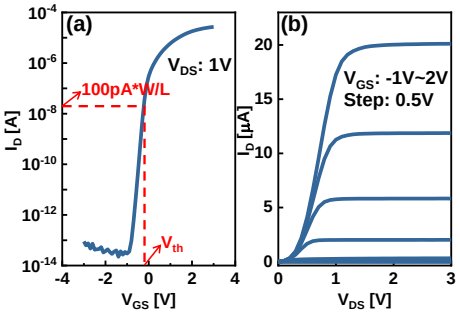

Figure 2. (a) Transfer and (b) Output curves of the fabricated IGZO FETs with W = 11μm and L = 70nm. Threshold voltage (V_{th}) is defined as the V_{GS} corresponding to I_D = 100pA * W/L in the transfer curve.

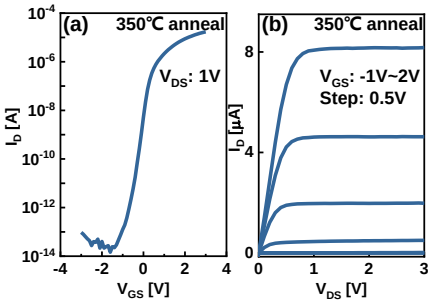

Figure 3. (a) Transfer and (b) Output curves of the fabricated IGZO FETs (W = 11μm, L = 70nm) after 350°C annealing treatment.

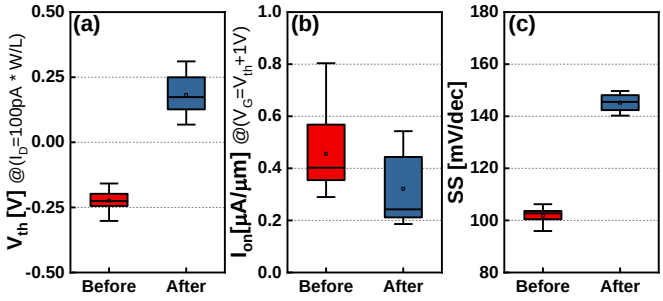

Figure 4. Comparison of (a) V_{th}, (b) W-normalized I_{on} (defined as the W-normalized I_D corresponding to V_{GS} = V_{th} + 1V) and (c) SS extracted from IGZO FETs before and after annealing at 350°C.