Monday Morning, August 5, 2024

Plenary Session
Room Hall 5A - Session PS-MoM

Plenary Session

Moderators: Markku Leskelä, University of Helsinki, Finland, **Mikko Ritala**, University of Helsinki, **Fred Roozeboom**, University of Twente and Carbyon B.V., The Netherlands, **Dmitry Suyatin**, AlixLabs A.B.

8:45am **PS-MoM-1 ALD Welcome and Introductory Remarks***, Mikko Ritala, M. Leskelä,* University of Helsinki, Finland

9:00am **PS-MoM-2 Opening Remarks: 50 Years of ALD***, Tuomo Suntola*, ., Finland **INVITED**

9:15am **PS-MoM-3 ALD: A Disruptive Technology Enabling New Device Architectures***, Ivo Raaijmakers,* ASM, Netherlands **INVITED**

For 3 decades ALD has been a crucial technology for scaling in the semiconductor industry. Many new device architectures, such as FinFET, Gate-All-Around, VNAND, and High Aspect Ratio DRAM can only be made by using the differentiated capabilities of ALD and PEALD, being conformality, uniformity, composition control, and relatively low process temperatures. Through academic and industrial R&D the materials capability and productivity of ALD and PEALD has been further improved which has caused the number of ALD layers in a chip to increase exponentially. This market pull - technology push tandem has propelled the ALD and PEALD market to grow to be among the largest deposition segments. In this presentation these developments will be reviewed, and a vision will be offered what is to come in the next decade for this pivotal technology for the semiconductor industry.

10:00am **PS-MoM-6 ALD 2024 Innovator Awardee Talk*: To Grow and* Not To Grow: Exploring Mechanisms during Atomic Layer Deposition***, Annelies Delabie***,** imec and KU Leuven (University of Leuven), Belgium **INVITED**

Electronic devices have become indispensable in our society as they affect important sectors such as communication, healthcare, education, transport, and energy. The expanding computing power and memory result from a spectacular evolution from planar micro-electronic devices to 3D nano-electronic devices. Today, the industry is moving to a transistor design that consists of stacked nanosheet channels and we are researching an even more complex geometry where the negative and positive channels are stacked on top of each other; the so-called complementary field effect transistor (CFET). To achieve the latter, we need to create semiconductor, dielectric, and metal patterns with nanoscale thickness and precision on horizontal and vertical sides of 3D structures.

Atomic layer deposition (ALD) is and will remain an enabling technique in electronic device fabrication. The cyclic process based on self-limiting surface reactions of gas phase precursors provides inherent growth control below the nanoscale and excellent conformality. A valuable emerging capability is to grow material only where needed, on a given area of a patterned substrate by area-selective ALD, which has great potential to improve or simplify the device fabrication. One key aspect for realizing (sub-)nanometer-thin continuous layers as well as area-selective deposition is the reactivity of the initial surface. The predominant process during ALD is fast precursor adsorption. Still, the initial substrate surface may react differently than the ALD grown material. When it is less reactive, it may not be covered after the first ALD cycle, and several cycles may be needed to close the layer. During this initial nucleation and growth regime, the changing surface composition affects the deposition by a complex interplay of processes, providing challenges and opportunities to modulate growth.

Rational process design based on mechanistic understanding can enable modulations from continuous nanometer-thin layers to sparse nanoparticles to area-selective deposition. This presentation therefore discusses mechanisms during the initial stages of ALD and area-selective ALD of dielectrics, conductors, and 2D materials. Experiments combined with modeling reveal various growth evolutions for different processes and substrates. On surface areas with low surface energy, adsorption may compete with surface diffusion and aggregation of adspecies. Diffusion can be leveraged to enhance selectivity on patterns with nanoscale dimensions. For 2D materials, understanding enables tuning the crystal size, location, and ultimately crystal shape and orientation, an exciting outlook for emerging devices and other applications.

11:00am **PS-MoM-10 ALE Welcome and Introductory Remarks***, Fred Roozeboom,* University of Twente and Carbyon B.V., The Netherlands*; D. Suyatin,* AlixLabs A.B., Sweden

11:15am **PS-MoM-11 Atomic Layer Precision Process to Enable Advanced Patterning toward High-NA EUV Era***, Eric Liu,* Tokyo Electron America **INVITED**

As the semiconductor industry aims to achieve higher resolutions in device patterning, the need for advanced lithography techniques becomes more imperative. Extreme ultraviolet (EUV) lithography is a promising solution with high-resolution capabilities to resolve the projection pattern on the wafer. Next-generation high-NA (numerical aperture) EUV lithography further enhances the imaging resolution to a smaller feature size. Still, the conventional plasma etching methods have presented challenges regarding pattern transfer from the lithography. Atomic layer precision etches, such as atomic layer etch (ALE), is a needed technology for EUV pattern transfer, as it can deliver high precision by controlling the pattern variations and etching selectivity with minimal damage to the masking/underlying material.

In this study, we investigate the effectiveness of these etching techniques for both EUV single exposure and double patterning applications. In EUV single exposure, atomic precision etching provides a high degree of control over critical dimension uniformity and pattern transfer fidelity. Using a combination of the ALE concept and advanced plasma species control, we demonstrate the ability to achieve high selectivity among challenging materials such as the photoresist and underlaying material and improve the pattern variation.

In EUV double patterning, our challenges are quite different from the EUV single exposure. The two unique challenges are [1] aggressive critical dimension shrink from lithography to etch and [2] narrow spacing issues. The atomic precision etching techniques offer a pathway to pitch splitting and pattern multiplication while maintaining high resolution and low line edge roughness. We present a novel approach based on alternative selective and anisotropic etching cycles to achieve pitch division with atomic precision when the space of the feature is under 10 nm. Overall, our results demonstrate the significant potential of atomic layer precision etch in enabling the development of advanced lithography techniques for next-generation semiconductor devices.

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