Atomic Layer Etching
Room Hall 3F - Session ALE-MoA

ALD+ALE and Emerging Topics in ALE

Moderators: Robert Clark, TEL Technology Center, America, LLC, **Dmitry Suyatin**, AlixLabs A.B.

4:00pm **ALE-MoA-11 Highly Selective Si Vertical Etching Enabled by Atomic-Level Process Utilizing $SiCl_4$ Plasma-Induced Selective Deposition***, **Miyako Matsui**,* Hitachi, Ltd., Japan*; M. Miura, K. Kuwahara,* Hitachi High-Tech Corp., Japan **INVITED**

Although the physical limitation of CMOS scaling is approaching, the local cell size of logic devices has still been continuously shrinking to improve the degree of integration. The patterning technology using extreme ultraviolet (EUV) lithography is one of key technologies for boosting pitch scaling. In addition, design technology co-optimization (DTCO) is another technology to boost cell size scaling, which enhances scaling by introducing various self-aligned processes. However, process challenges exist for both technologies. Etching processes using thin EUV resists, which needs to be thinner to accommodate the decrease in the depth of focus of EUV lithography, require extremely high selectivity and precise control of critical dimensions. Selective etchings for DTCO require high selectivity between layers having a similar material composition. In both cases, selective deposition for forming protective layers only on unetched materials can solve these process challenges and achieve extremely highly selective etchings.

In this study, we investigated a plasma-induced selective deposition process using a microwave-ECR etching system for forming a protective layer on top of the mask. A deposition layer was formed only on SiO_2 masks without forming an unnecessary deposition layer on Si surfaces of etching area, such as bottoms of the patterns and isolated etching area. This process effectively achieves extremely highly selective etchings by selectively forming the protective layers prior to the etching procedure in the same chamber.

We suggested a process for selectively forming protective layers on a SiO_2 without forming on a Si etching area by using a $SiCl_4/H_2/Cl_2$ plasma. On the Si surface, adsorbed $SiCl_x$ easily desorbed again by reacting with Cl generated from the plasma. On the other hand, adsorbed $SiCl_x$ on SiO_2 was thought to be more difficult to desorb by reacting with Cl due to Si-O having larger binding energy than Si-Si. After the deposition layer was selectively formed on the SiO_2 mask, the layer was oxidized using an O_2 plasma treatment to improve the etching resistance during the Si-etching. The O_2 plasma treatment time was controlled not to prevent the Si substrate from being etched during the Si-etching.

Finally, we demonstrated the selective deposition to etch a line-and-space pattern with a SiO_2 mask. In this process, selective deposition, oxidation, and Si etching were cyclically carried out. The extremely highly selective etching was achieved using the atomic-level selective deposition process without forming an unnecessary deposition on an isolated Si area.

4:30pm **ALE-MoA-13 Quasi-ALE Process Transfer from Lab to 300mm Line and Its Optimisation***, **Jenefa Kannan**, M. Rudolph,* Fraunhofer IPMS-CNT, Germany*; R. Jam, A. Karimi, D. Suyatin, J. Sundqvist,* AlixLabs, Sweden

Atomic layer etching (ALE) has found its place in advancing technologies as chip sizes continue to shrink and pitch sizes get smaller. The ALE process offers several advantages over conventional reactive ion etching (RIE) such as better directionality, uniformity, selectivity and damage free surface after etching [1,2]. A self-limited removal of material with minimal damage to the surface requires a good control over every step of the ALE process [3]. Quasi atomic layer etching (QALE) is defined as a process when more than one mono-layer of the material is etched per cycle. Surface treatment, Control of ion energies and appropriate evacuation of the chemical component (Cl_2) is necessary to control the etch rate per cycle and achieve etch saturation in a cycle sweep.

In our work, we have conducted in-depth studies to set up a molecular QALE process as seen in Figure 1 at our 300 mm facility in an inductively coupled plasma (ICP); decoupled plasma source (DPS) AMAT chamber on 350 nm amorphous Silicon (aSi) which was deposited on 12" blanket wafers. First, experiments were conducted to establish the bias power and pressure window. After this step, Ar sputter threshold for amorphous Silicon was determined. This was used as baseline to setup a cyclic process where the EPC was determined over low ion energies by optimising the bias power and activation time during exposure to Ar plasma. Damage or roughness caused to the layer being etched severely degrades device performance with decreasing dimensions [4]. Hence, to investigate the same, an Ellipsometer model was developed to understand the composition and thickness of this rough layer of the aSi surface post QALE etch. Thickness of the rough layer was evaluated over increasing number of cycles. The EPC for different Ar activation times at bias power 25 W is shown in Figure 2. The thickness of the rough layer at the end of the cycles is seen in Figure 3. We observed that the Ar activation time and no. of cycles have an influence on the thickness of the rough layer after etching.

In this work we investigate the factors and challenges that need to be taken into consideration while transferring the ALE process from lab to fab.In general, our work highlights the importance of control of every step in QALE for effective transfer and commercial viability in a 300mm line.

4:45pm **ALE-MoA-14 Deposition and Etchback Approach for Ultrathin ZrO_2 Coatings on TiO_2/ZrO_2 Core/Shell Nanoparticles***, J. Sempel, M. Kaariainen, T. Colleran,* University of Colorado at Boulder*; A. Lifschitz,* Meta Reality Labs*; **Steven George**,* University of Colorado at Boulder

Atomic layer deposition (ALD) and atomic layer etching (ALE) techniques were used to deposit and etchback a thin ZrO_2 shell on TiO_2/ZrO_2 core/shell nanoparticles. Possible pinholes in the initial ZrO_2 shell on the TiO_2/ZrO_2 core/shell nanoparticles were minimized by first growing thicker ZrO_2 films by ZrO_2 ALD. These thicker ZrO_2 ALD films were then etched back to produce thinner more continuous ZrO_2 films. The ALD and ALE were performed while the nanoparticles were agitated using a rotary reactor. ZrO_2 ALD films were deposited using sequential, self-limiting exposures of tetrakis(dimethylamino) zirconium (TDMAZ) and H_2O. Self-limiting conditions for the ZrO_2 ALD were determined by monitoring the pressure during multiple micropulses of the ALD reactants. *Ex situ* analysis of the nanoparticles was performed using transmission electron microscopy (TEM) to observe the growth of the ZrO_2 shell on the core/shell TiO_2/ZrO_2 nanoparticles. The ZrO_2 ALD led to more spherical ZrO_2 shells on the crystalline and more irregular TiO_2 cores in the absence of nanoparticle aggregation. The ZrO_2 ALD on the nanoparticles had a growth rate of 1.1 Å/cycle. Tunable ZrO_2 coatings were observed with thicknesses ranging from 5 nm to 25 nm after up to 250 ZrO_2 ALD cycles. The ZrO_2 deposited film was then etched back using sequential HF and $TiCl_4$ exposures. Self-limiting conditions for the ZrO_2 ALE were again determined by monitoring the pressure during multiple micropulses of the ALE reactants. Quadrupole mass spectrometry (QMS) experiments also identified $ZrCl_4$ etch products and TiF_xCl_y ligand-exchange products during the $TiCl_4$ exposures. *Ex situ* TEM studies revealed that the spherical ZrO_2 shells were maintained during the ZrO_2 ALE with no observable nanoparticle aggregation. The ZrO_2 ALE on the nanoparticles had an etch rate of 6.5 Å/cycle. Tunable ZrO_2 coatings were produced by the ZrO_2 ALE from 25 nm back down to 5 nm using 30 ZrO_2 ALE cycles. This procedure employing ZrO_2 ALD and ZrO_2 ALE provides exceptional control over the ZrO_2 shell thickness and quality on the TiO_2/ZrO_2 core/shell nanoparticles.

5:00pm **ALE-MoA-15 Study of Depositing Si_3N_4 on Si Wafers Using PEALD and Atomic Scale Removal of Underlying Native Oxide Using PAALE in the Same Chamber Without Ion Bombardment Damage***, **Birol Kuyel**, A. Alphonse, J. Alex,* Nano-Master

The mitigation of substrate damage is crucial to any process at the atomic scale (1). This is especially true for device technology applications in which source/drain and metalized regions are susceptible to damage (2). To eliminate substrate damage, we have developed plasma-enhanced atomic layer deposition (PEALD) of silicon nitride without ion bombardment (3).

The removal of native oxide on the Si wafer before depositing Si_3N_4 is also important for device performance (4). Removing the native oxides from the Si wafer using other means, such as reactive ion etching or wet etching, results in substrate damage and defects to the wafer.

Here, we will discuss the means of removing the native oxide from the Si wafer surface using Plasma Assisted Atomic Layer Etching (PAALE) prior to depositing silicon nitride. The PAALE process occurs in the same PEALD chamber, which prevents re-oxidation between steps. Furthermore, studies will be presented on the prevention of ion flux damage on the substrate surface with controlled ion energies and the possibility of performing PAALE without the incidence of any ions. The objective of the study is to develop a tool that can perform angstrom-precise PEALD and PAALE processes in the same chamber and prevent substrate damage.

References:

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2. C. Petit-Etienne, M. Darnon, L. Vallier, E. Pargon, G. Cunge, F. Boulard, O. Joubert, S. Banna and T. Lill, J. Vac. Sci. Technol. B 28 (5), 926-934 (2010)
3. US Patent # 9,972,501 B1 May 15, 2018
4. Dominik Metzler, Chen Li, C.Steven, "Investigation of Thin Oxide Layer Removal from Si Substrates Using an SiO2 Atomic Layer Etching Approach: The Importance of the Reactivity of the Substrate"

5:15pm **ALE-MoA-16 N-Heterocyclic Carbenes for Area Selective Atomic Smoothing***, **Eden Goodwin**,* Carleton University, Canada*; M. Davies, P. Ragogna, M. Karttunen,* Western University, Canada*; S. Barry,* Carleton University, Canada*; C. Crudden,* Carbon To Metal Coating Institute / Queens University, Canada

High-volume manufacturing of microelectronics relies on thousands of sequential patterning, deposition, etch, and surface smoothing steps to create integrated circuits comprised of interwoven metallic, semiconducting, and dielectric features. Throughout the fabrication process, surface roughness is carefully monitored to ensure proper adhesion between layers and maximize distance between features. If surface roughness exceed tolerance limits, films are more likely to delaminate and manufactured features are more like to short-circuit.[1] At sub-nm feature sizes these tolerances become more challenging to reach.

Current smoothing techniques either rely upon top-down mechanical polishing[2] or on plasma methods.[3] Both techniques preferentially etch surface features, leaving a process gap for targeted surface smoothing on complex architectures. In pursuit of a more accessible smoothing methods compatible with complex architectures, we have identified a vapor phase method for smoothing gold surfaces using a known area selective small molecule inhibitor.[4] We explore the kinetics of adsorption and desorption of a N-heterocyclic carbene (NHC) through in-situ quartz crystal microbalance (QCM) analysis and molecular dynamics (MD) simulations. QCM traces (Fig. 1) show a saturative growth behavior for the initial dose of NHC achieving a surfactant density of 97 ng cm^{-2}, while subsequent doses saturate to 60 ng cm^{-2}. These differences are attributed to a reduction in the total number of available surface sites through atomic smoothing.

To confirm this, changes in surface roughness were analyzed through atomic force microscopy (AFM). AFM images (Fig.2) show a significant reduction in calculated root-mean-square (RMS) roughness values between surfaces left untreated (2.97 nm), heated under vacuum (2.38 nm) and those treated with NHC heated under vacuum (1.87 nm).

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