

Area Selective ALD

Room Hall 3E - Session AS-MoA

Selective ALD by Area-Deactivation

Moderator: Prof. Dr. Stacey Bent, Stanford University

4:00pm **AS-MoA-11 Revealing New AS-ALD Chemistries with Ab Initio Approaches: From Interpretation to Prediction**, Ralf Tonner-Zech, Leipzig University, Germany

INVITED

Area-selectivity is currently one of the key challenges in atomic layer deposition. The selectivity observed stems from different surface reactivities of precursors and - for inhibitor-based approaches - the inhibitor molecules. Ab initio approaches like density functional theory can help to reveal the key mechanisms underlying this selectivity. They thus help to understand experimental findings in the first step (interpretation). In the second step, theory can ideally provide design principles for inhibitors and precursors from detailed analysis of several systems (prediction). I will present our progress in both areas: (i) interpretation of new AS-ALD reactivities for small molecule inhibitor-(SML)-based approaches to ALD on dielectric and metallic surfaces,[1] and (ii) understanding of design principles for SMLs and precursors using ab initio computations and electronic structure analysis.

[1] J. Yarbrough, F. Pieck, A. B. Shearer, P. Maue, R. Tonner-Zech, S. F. Bent, *Chem. Mater.* 2023, 35, 5963–5974; (b) J. Yarbrough, F. Pieck, D. Grigjanis, I.-K. Oh, P. Maue, R. Tonner-Zech, S. F. Bent, *Chem. Mater.* 2022, 34, 4646–4659; (c) S. Zoha, F. Pieck, B. Gu, R. Tonner-Zech, H.-B.-R. Lee, in revision.

Funding from a Merck KGaA, Darmstadt, Germany 350th Anniversary Research Award is gratefully acknowledged.

4:30pm **AS-MoA-13 Area Selective Atomic Layer Deposition Using a Size Cutter**, Han-Bo-Ram (Boram) Lee, Incheon National University, Republic of Korea

INVITED

Area-selective atomic layer deposition (AS-ALD) has received great attentions due to its potentials for a key toolbox in the nanofabrication of Si devices. The approach using inhibitor molecules which locally change surface chemical properties to inert toward the following ALD reactions has been widely used. The defect density of inhibitor layer which is a potential nucleation site should be minimized to achieve high selectivity, however, it is difficult due to the steric hindrance of inhibitor molecule during comparative adsorption. In this presentation, a simple approach to minimize the steric hindrance effects of inhibitor and maximize the blocking property is introduced. The ligand size of inhibitor layer could be reduced by only additional pulse of H₂O and the adsorption coverage of inhibitor could be increased. The concept of size cutter has been interpreted by using theoretical calculations with density functional theory (DFT) and Monte Carlo (MC) simulation and the results show highly consistency with experimental observation. The results could provide insights for the next generation nanofabrication in the semiconductor technology using AS-ALD.

5:00pm **AS-MoA-15 Ald Grown Self-Assembled Monolayers: Using Area-Selective Deposition to Characterize Molecular Scale Pinholes**, Sakari Lepikko, R. Ras, Aalto University, Finland

Area selective atomic layer deposition has become a key method for creating patterned thin film structures for various applications in the semiconductor industry. Self-assembled monolayers (SAMs) are often used for de-activating surfaces, to block the ALD film growth (Figure 1). SAMs allow easy patterning, are capable of inhibiting wide variety of precursors, and are suitable on various substrates. Whereas certain SAM chemistries, such as alkyl trichlorosilanes are good for de-activating oxide substrates, they are also notoriously difficult to grow defect free, thereby reducing the SAM effectiveness to block ALD growth.

A promising option is to grow the SAMs directly in the ALD reactor, as it provides dry vacuum environment with good temperature control, thus making it an ideal tool for optimizing the SAM growth. Here, we present how the quality of non-fluorinated octyltrichlorosilane SAMs can be tuned to better block growth of various ALD films with differently sized precursor molecules [1]. By increasing SAM growth time its areal coverage increases, which leads to reduction of pinholes in the SAM and thus to the adsorption sites for the ALD reactant molecules (Figure 2). We also show that the maximal pinhole size reduces with the increasing coverage, which helps blocking adsorption of smaller ALD precursor molecules such as diethyl zinc. We see that growing SAMs directly in an ALD reactor could provide

means to create more uniform SAMs with better resistivity against various ALD precursors, thus helping fabrication of even more demanding nanostructures in the semiconductor field.

We demonstrate that these SAMs have tunable hydrophobicity with extraordinarily low droplet friction. We demonstrate the world's most slippery surface by coating of SAM on black silicon.[1]

Lepikko, S., *et al.* Droplet slipperiness despite surface heterogeneity at molecular scale. *Nature Chemistry* (2024). <https://doi.org/10.1038/s41557-023-01346-3>

5:15pm **AS-MoA-16 Area-Selective Etching of Poly(lactic acid) via Hydrogenolysis for Self-Aligned ALD**, Valtteri Lasonen, M. Ritala, University of Helsinki, Finland

Our previous works have demonstrated that area-selective etching (ASE) of polymers is a novel approach for enabling self-aligned ALD.^{1,2} In ASE, a polymer film is decomposed only on catalytic surfaces whereas on non-catalytic surfaces the polymer stays intact. ASE was demonstrated in the air using Pt as the catalytic and native SiO₂ as the non-catalytic surface with two polymers, polyimide and poly(methyl methacrylate) (PMMA). After the ASE of polyimide, ALD-Ir grew only on the exposed Pt surface, whereas no growth was observed on the polyimide. In the case of ASE of PMMA, small amount of ALD-Ni growth occurred also on PMMA. However, a simple lift-off after the ALD removed the unwanted Ni. Other catalytic surfaces were also identified, such as CeO₂. Furthermore, it was demonstrated that only a small amount of ALD-Pt or ALD-CeO₂, even down to a fraction of a monolayer, was enough to show a clear catalytic effect. This means that small amounts of Pt can be deposited on a metal surface, and CeO₂ on an insulator surface, to catalytically activate them. This is important because neither Pt nor CeO₂ is commonly used in semiconductor devices.

Many materials used in semiconductor devices are prone to oxidation when heated in the air, thus, non-oxidative atmospheres must be found for ASE. Two such atmospheres, inert (99.999% N₂) and H₂ (5% H₂ in Ar), were tested with PMMA and polyimide.^{1,2} Out of all the surfaces tested only Ti, Pd, and Cu showed some catalytic effect in the inert atmosphere and/or in the presence of H₂. For example, the well-known hydrogenolysis catalyst, Pt, did not show any catalytic effect on the decomposition of PMMA in the presence of H₂. This is most likely because PMMA is not susceptible to hydrogenolysis, unlike condensation polymers, such as poly(lactic acid) (PLA). Here, we demonstrate that PLA is catalytically decomposed on several known hydrogenolysis catalysts, such as Pt, Ir, and Ni in the presence of H₂ whereas in the inert atmosphere PLA films stay intact on these surfaces at the same temperatures. Additionally, Co is demonstrated to work as a catalytic surface also in the inert atmosphere. In this case the removal mechanism is catalytic cracking of the polymer. These new findings give us confidence that ASE of polymers is possible with plethora of different surface combinations by carefully choosing the right catalytic material, polymer, and atmosphere, thus allowing new self-aligned ALD processes.

References

1. Zhang et al. *Coatings*. **2021**, 11(9), 1124.
2. Lasonen et al. *Chem. Mater.* **2023**, 35(15), 6097–6108.

5:30pm **AS-MoA-17 Selective Surface Fluorination to Enable ASD of Polymer and Metal Oxide on SiN vs. SiO₂**, Jeremy Thelven, H. Oh, H. Margavio, C. Oldham, G. Parsons, North Carolina State University

3D integration of semiconductor devices such as Gate-All-Around FETs and vertical device stacking is being implemented to reduce power consumption and enable further scaling for logic and memory devices.¹ There is a critical need to reduce the processing budgets to achieve such advanced designs and area-selective deposition (ASD) offers a bottom-up approach to achieve the desired scaling goals.² The ability to selectively react and deposit on an oxide vs nitride surface is widely recognized as key roadblock for scaling due to the chemical similarity of these surfaces. ASD on nitride vs oxide surfaces, or vice versa will provide new options for patterning, to improve self-alignment, and to reduce edge placement errors. In this work, we demonstrate the use of a selective surface fluorination treatment to promote ASD on SiN vs. SiO₂.

To demonstrate ASD on SiN vs. SiO₂, we explored a surface treatment using molybdenum hexafluoride (MoF₆) on blanket SiN and SiO₂ wafers. Next, we deposited about 50nm of polypyrrole (PPy) CVD on both surfaces. We found that PPy proceeded to grow as a film on the SiN surface after a brief nucleation delay, while only showing isolated nuclei on the fluorinated SiO₂ surface. As a further demonstration, experiments were performed on patterned SiO₂/SiN wafers which further confirmed PPy selective growth.

Monday Afternoon, August 5, 2024

We believe the MoF₆ exposure leads to the fluorination of both surfaces, which was confirmed by XPS, where this fluorination selectively passivates PPy growth on the SiO₂ surface. To extend this demonstration of ASD on SiN vs SiO₂ to other types of materials, we recently tested the treatment with the deposition of TiO₂ through ALD. We found that this selective fluorination passivation of the SiO₂ surface allows for selective growth of TiO₂ on SiN. The mechanisms behind selectivity, and the extent of passivation are currently under investigation by our group.

1 Datta, S.; Dutta, S.; Grisafe, B.; Smith, J.; Srinivasa, S.; Ye, H. Back-End-of-Line Compatible Transistors for Monolithic 3-D Integration. *IEEE Micro* 2019, 39 (6), 8–15. <https://doi.org/10.1109/MM.2019.2942978>.

2 Decadal Plan for Semiconductors. Semiconductor Research Corporation. <https://www.src.org/about/decadal-plan/>

Author Index

Bold page numbers indicate presenter

— L —

Lasonen, V.: AS-MoA-16, **1**

Lee, H.: AS-MoA-13, **1**

Lepikko, S.: AS-MoA-15, **1**

— M —

Margavio, H.: AS-MoA-17, **1**

— O —

Oh, H.: AS-MoA-17, **1**

Oldham, C.: AS-MoA-17, **1**

— P —

Parsons, G.: AS-MoA-17, **1**

— R —

Ras, R.: AS-MoA-15, **1**

Ritala, M.: AS-MoA-16, **1**

— T —

Thelven, J.: AS-MoA-17, **1**

Tonner-Zech, R.: AS-MoA-11, **1**