ALD Applications
Room Hall 3D - Session AA2-MoA

Applications in ULSI FEOL: Gate Electrodes & Contact Metals, High-K, and 3D Transistor Fabrication

Moderators: Scott Clendenning, Intel Corporation, **Christian Wenger**, IHP - Leibniz Institut fuer innovative Mikroelektronik

4:00pm **AA2-MoA-11 Thermal Atomic Layer Deposition of Boron Containing Oxide Films as Solid Sources for Doping of Advanced Memory Devices**, *Y. Shen,* Beijing Superstring Academy of Memory Technology, China*; S. Yang,* Institute of Microelectronics, China*;* ***Jinjuan Xiang****,* Beijing Superstring Academy of Memory Technology, China*; J. Liu, J. Gao,* Institute of Microelectronics, China*; G. Wang, C. Zhao,* Beijing Superstring Academy of Memory Technology, China

In recent decades,with the continuous scaling downof devicedimensionsand the emergence of complex three-dimensional structures,conventional ion implantation cannot meet the requirements of non-damage and uniform doping of the nonplanar transistor architecture. Atomic layer deposition (ALD) is one of the mostpromising methods for forming controlled and conformal dopant-containing layer. Compared to plasma enhanced ALD, thermal ALD has better ability for achieving the required conformity conditions and high scalability for 3D structures with higher AR ratio. By combing of ALD with the heat-driven annealing,non-damage and conformal doping in Si can be achieved. However, ALD doping still faces many challenges, one of the big issues is that B_2O_3 films cannot grow sustainably, which hinders its further application [1, 2].

In this paper, Al_2O_3 and SiO_2 layer were used as enhance layer to promote the deposition of B_2O_3 by thermal ALD. By using Al_2O_3 interlayer, low lewis acidity of Al−OH- was formed. Boron is evenly distributed in $B_xAl_{1-x}O_y$ film with a content of about 15 at. %, which is higher than that in $B_xSi_{1-x}O_y$ film. After rapid thermal annealing, the maximum doping concentration of B can reach 2E20 atom /cm^3, and the doping concentration of Al in Si is low. When SiO_2 as the enhance layer, the maximum B doping concentration is 3E19 atoms /cm^3. In addition, the content of B in $B_xSi_{1-x}O_y$ film and doping concentration in Si are higher at low B:Si ratio of 4:3 than at B:Si of 5:1, which is mainly due to the fact that enough SiO_2 layer can promote the growth of B_2O_3 more effectively. Uniform and dose-controlled doping achieved by this thermal ALD doping is believed to have great application prospects in 3D structures device, especially for vertical stacked dynamic random-access memory (DRAM).

4:15pm **AA2-MoA-12 Plasma-Enhanced ALD of Thin Conductive Cu Films**, ***Maria Gabriela Sales****, N. Nepal, P. Litwin, D. Boris, S. Walton, V. Wheeler,* U.S. Naval Research Laboratory

Interconnect vias are conduits that transport signals between circuit components, and are typically made of Cu due to its low resistivity, high thermal conductivity, low coefficient of thermal expansion, high melting temperature, and good mechanical properties. Traditionally, Cu interconnect vias are fabricated through electrochemical deposition which is followed by chemical mechanical polishing and various cleaning steps to get the Cu mostly conformal with the via structure. However, these processes tend to leave behind voids in the via and/or leftover Cu in areas with unwanted Cu growth. Atomic layer deposition (ALD) is a promising alternative technique to avoid such reliability issues because it is a saturating and self-limiting deposition process. Furthermore, the layer-by-layer nature of ALD allows for precise thickness control, which is an important consideration in the scaling of circuit components.

For proper implementation of ALD in the deposition of via structures, we need to study the key ALD processing conditions that produce Cu thin films with the desired chemical and physical properties and optimal electrical performance. In this work, we study a plasma-enhanced Cu ALD process in a Veeco Fiji G2 reactor equipped with a turbo pump and substrate biasing, using copper(I)-N,N'-di-sec-butylacetamidinate, or $[Cu(^sBu\text{-}amd)]_2$, as our Cu precursor and H_2 plasma as our reducing reactant. We present a parametric study where we investigate the different growth conditions, i.e., growth temperature, precursor pulse, composition of gases in the plasma, and plasma power, among others, and observe how they affect Cu film growth. In-situ ellipsometry is used to monitor growth rate, post-deposition X-ray photoelectron spectroscopy (XPS) is used to analyze the film and interface chemistry, and atomic force microscopy (AFM) is used to examine the resulting film morphology. Initial results show metallic Cu films were successfully deposited using a 300 W Ar/H_2 plasma with a 20% Ar flow fraction and a 10-second plasma pulse duration. This demonstrates the feasibility of this PEALD Cu process; however, to-date films are limited in thickness, and possible approaches to overcome these issues will be discussed.

4:30pm **AA2-MoA-13 Selective Atomic Layer Deposition of Ultra-Thin Ru on W for Metal Contact**, ***Rong Chen****, Z. Qi, E. Gu,* State Key Laboratory of Intelligent manufacturing Equipment and Technology, School of Mechanical Science and Engineering, Huazhong University of Science and Technology, China*; B. Shan,* State Key Laboratory of Materials Processing and Die & Mould Technology, School of Materials Science and Engineering, Huazhong University of Science and Technology, China*; K. Cao,* State Key Laboratory of Intelligent manufacturing Equipment and Technology, School of Mechanical Science and Engineering, Huazhong University of Science and Technology, China

Atomic selective area layer deposition (ASD) of ruthenium has attracted considerable interest for various applications in nanoelectronics and due to its potential role in front-end-of-line (FEOL) contact in future technology nodes. In this talk, it provides insight into the effects of discrete feeding atomic layer deposition (DF-ALD) process and post-processing treatments on the nucleation of Ru film and selective growth on W/SiO2. DF-ALD process can improve the purging of excess physically adsorbed precursors, provide more reaction sites, and increase the nucleation density. With DF-ALD, ultra-thin and low-resistivity Ru thin film on W contact was obtained. According to KMC theoretical calculations, when there are excess physical adsorption precursors and chemically adsorbed reaction by-products around the reaction site, there is a lack of steric hindrance required for chemical reactions and the reaction is difficult to occur. Due to the size-dependent mobility of nanoparticles and differences in substrate adsorption energy, post-processing more easily promotes nucleation defects in non-growth areas migration to the growth area. It is an effective way to eliminate non-growth area defects and amplify selectivity. The inherently selective ALD process is successfully transferred onto W/TiN/SiO_2 nanopatterns with ~100 nm pitch and obtained high selectivity with 5–6nm films on W and no defects in the SiO_2 and TiN regions. The results indicate that inherently selective ALD is a robust and general tool that has excellent application prospects in FEOL processes, which provides an innovative avenue for self-aligned nanostructures.

4:45pm **AA2-MoA-14 Effect of High Precursor Dose on the IZO Film Property Uniformity Within Wafer Deposited by Thermal ALD**, ***Yuting Chen****, P. Yuan, X. Ma, Z. Jiao, Y. Shen, L. Chai, J. Xiang, M. Zeng, H. Sun, G. Wang, C. Zhao,* Beijing Superstring Academy of Memory Technology, China

Recently, IGZO-based vertical channel-all-around (CAA) thin-film transistors (TFT) for 2T0C dynamic random access memory (DRAM) with better density advantages has attracted wide attention. Zinc-doped In_2O_3 (IZO)is a potential gate electrode material for CAA TFT device, because of its relatively low resistivity, and low process thermal budget, which is perfectly suitable for IGZO-based devices. IZO material property deposited by ALD on 12-inch wafer has been rarely studied. Usually, to achieve better step coverage on high aspect ratio (AR) vertical structure, higher precursor dose is necessary, compared with the saturation dose obtained on planar structure. Hence, in this work, thermal ALD IGZO/Al_2O_3/IZO film stack, which simulated the gate stack in CAA TFT device, were employed as the vehicle to investigate the IZO film property at high precursor dose. Moreover, the samples of precursor inlet and outlet regions were analyzed to reveal the film uniformity within 12-inch wafer. Unexpectedly, the IZO film of inlet region has the worse electrical properties. Materials characterization were conducted to elucidate the mechanism of heterogeneity. Although XPS results shows no difference in the In/Zn composition ratio between the inlet region and the outlet region, XRD results shows higher In_2O_3 crystallinity in inlet region than outlet region, which is also confirmed by AFM scans. Based on these results, it can be inferred that high-dose precursor at the inlet position may lead to insufficient ALD reaction process, resulting in many defects in the IZO film and degraded electrical properties. The non-uniformity of IZO film poses some challenges for subsequent process integration, such as the CMP process.

This work highlights the significant impact of different regions within 12-inch wafer on the properties of films at high dose. In spite step coverage can be improved by increasing the precursor dose, too much precursor will lead to degenerated film at inlet region.

5:00pm **AA2-MoA-15 Development of ALD Gate Dielectrics for TMD Nanosheet FETs**, *T. Lee, B. Chao, Y. Chung, Y. Su,* TSMC, Taiwan*; B. Liu, C. Su, C. Kei,* Taiwan Instrument Research Institute, Taiwan*; C. Cheng,* ***Pinyen Lin****, I. Radu,* TSMC, Taiwan

Superior electrostatics control of monolayer (1L) TMDs holds great potential in advancing the scaling of nanosheet (NS) transistors in advanced technology nodes [1]. One critical aspect is to achieve a conformal dielectric layer on TMD NS channel using atomic layer deposition (ALD) [2]. The main challenge in achieving high-quality gate dielectrics is forming a good nucleation layer on the dangling bond-free TMD interface. This study successfully used the ALD technique to form a uniform AlOx thin film on 1L-MoS2 without damaging the material. Furthermore, good performance of MoS2 NS nFET is also successfully demonstrated.

5:15pm **AA2-MoA-16 ALD in Semiconductor Logic Manufacturing: Challenges Met and Opportunities Ahead***, **David Towner***, Intel Corp. **INVITED**

Atomic Layer Deposition has played a unique, enabling role in the evolution of semiconductor logic device manufacturing.ALD's ability to bring atomic level control to thin film deposition is particularly critical to applications at the heart of transistor performance, such as High-K gate dielectrics and workfunction materials.With the progression to 3-D transistor structures like FinFETs and RibbonFETs, ALD's ability to conformally deposit on complex topography is unparalleled.This talk will present one industry expert's take on ALD's success stories as well as the many challenges ahead, including less glamorous but important factors such as cost and manufacturability.Special effort will be taken to highlight opportunities for further innovation as we continue to advance Moore's Law.

Author Index

Bold page numbers indicate presenter