

Atomic Layer Deposited Zr-doped HfO₂ (HZO) and Indium Gallium Oxide (IGO) Thin Films for 3D Gate-All-Around FeFET

Boncheol Ku¹, Jae Seok Hur², Jae Kyeong Jeong², and Changhwan Choi^{1,*}

¹Division of Materials Science and Engineering, Hanyang University, Seoul 04763, Korea

²Department of Electronic Engineering, Hanyang University, Seoul, 04763, Korea

Corresponding author: cchoi@hanyang.ac.kr

Recently, HfO₂-based ferroelectric (FE) field effect transistors (FeFETs) have gained attention for NAND flash memory applications due to their superior advantages compared to SiO₂/Si₃N₄/SiO₂ (ONO)-based FETs. These advantages include faster write/erase speeds, non-destructive readout, lower operation voltage, higher scalability, and CMOS compatibility. However, when FE thin films are applied to poly-Si, there can be issues such as grain-dependent threshold voltage (V_{th}) degradation and temperature-induced V_{th} instability due to the low-k interfacial layer formed at the interface between FE-HfO₂ and poly-Si. With this regard, materials system using suitable FE thin film and oxide semiconductor should be explored and corresponding device feasibility needs to be investigated. To address this, we have proposed using atomic layer deposited (ALD) FE thin film and oxide semiconductors (OS) as charge trapping layer and alternative channel, respectively, in 3D NAND architecture.

In this study, we successfully demonstrated ALD Zr-doped HfO₂ (HZO) FE thin film and an indium-gallium oxide (IGO) channel for a 3D vertical Gate-All-Around (GAA) NAND flash memory device using with gate length (L_g) and spacer length (L_s) of 50 nm. [Fig. 1] These FE and OS thin films are adopted as an alternative charge trapping layer and channel layer alternative ONO and poly-Si, respectively. The I_d - V_g characteristic of the 3D GAA FeFET device indicates high-quality interface between the HZO and IGO thin films, with subthreshold swing of 90 mV/dec and almost no hysteresis under bias sweeping. The device shows a maximum memory window (MW) of 2.5 V, allowing for potential multilevel cell (MLC) operation. The stable sub-loop switching of ferroelectricity for MLC memory operation is an important factor, and stable 2 bits/cell retention properties up to 10⁴ sec at room temperature are achieved, extrapolated to 10 years retention time. [Fig. 2]. These results suggest that ALD FE thin film and OS materials can be a promising alternative to current ONO/poly-Si materials for advanced V-NAND flash memory applications.

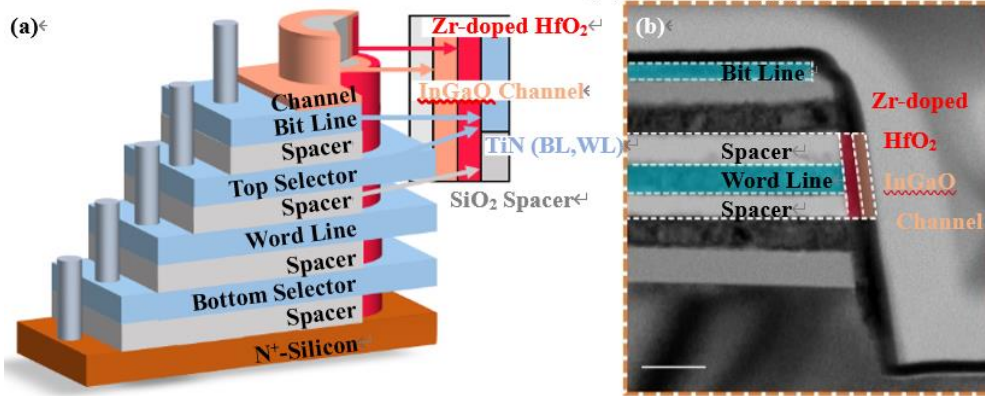


Figure 1. (a) Schematics of 3D GAA FeFET device with ALD FE HZO and IGO thin films, and (b) HR-TEM cross-sectional image of the corresponding 3D GAA FeFET device.

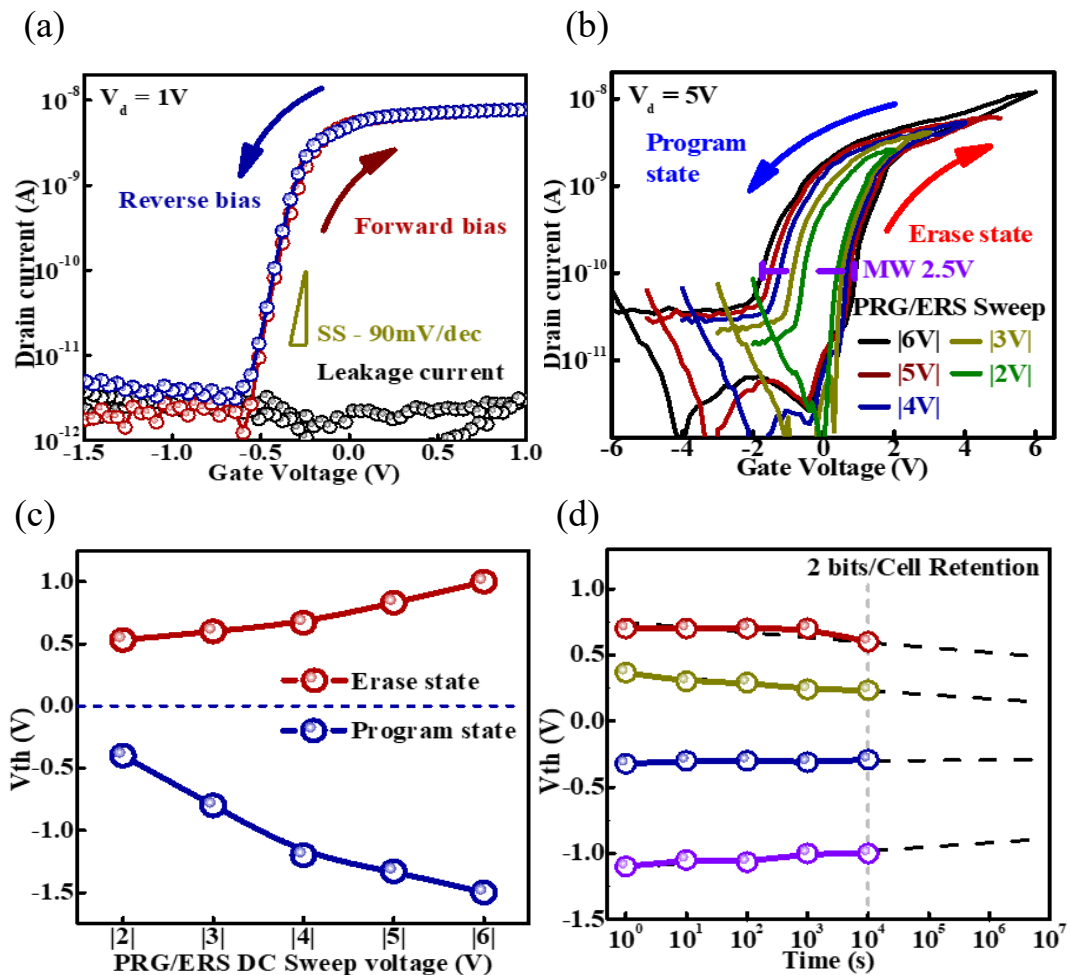


Figure 2. (a) I-V curve of a word line. SS of 90mV/dec was observed with negligible leakage current. (b) Hysteresis behavior during voltage scan with $V_d = 5V$, where MW of 2.5V was extracted. (c) Comparison of V_{th} for program/erase states according to word line voltage scan from (b). As a result, V_{th} change of erase state is less sensitive to the voltage amplitude compared to program state. (d) Retention for 2bits/cell was measured up to 10^4 sec at RT and expected for the 10 years.