

Figure 1. (a) Schematic cross-section, (b) optical image, and (c) device layout of the fabricated VTFTs with SiO₂ vertical sidewall and ALD IGZO channel. Channel width and length were designed to be 20 and 150 nm, respectively.

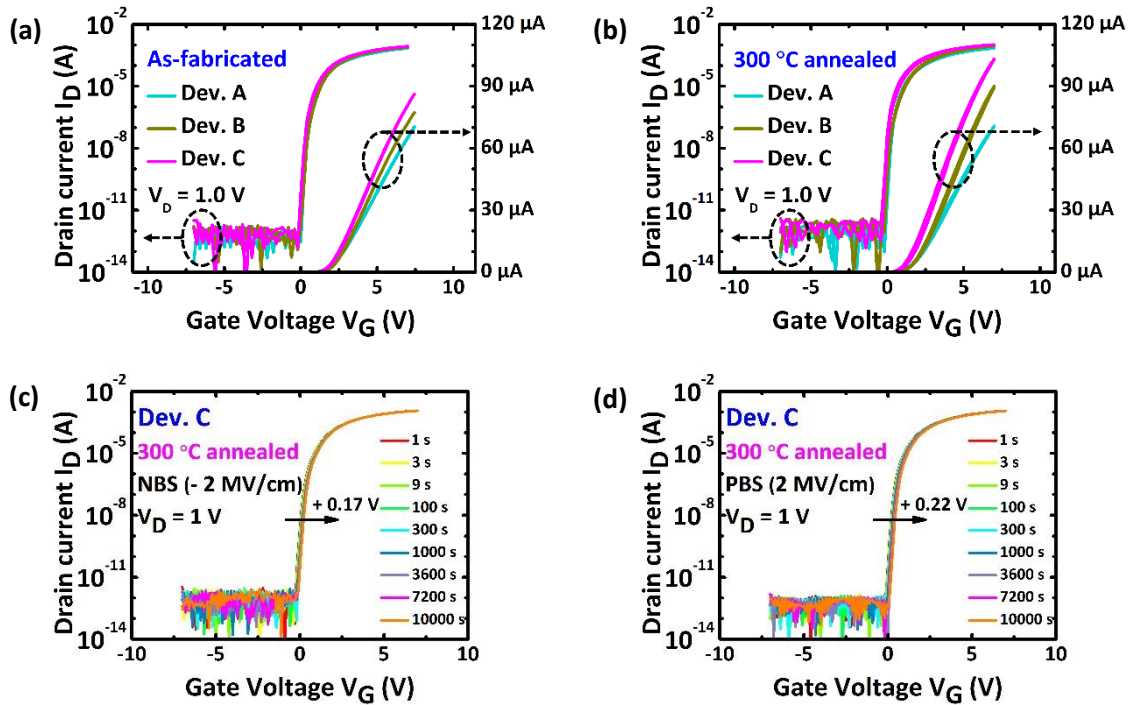


Figure 2. Transfer characteristics of the ALD IGZO VTFTs fabricated with different T_D 's (a) before and (b) after the post-annealing process at 300 °C. Variations in transfer curves of the Dev. C with stress time evolution under the (c) negative-bias stress (NBS) and (d) positive-bias stress (PBS) conditions.

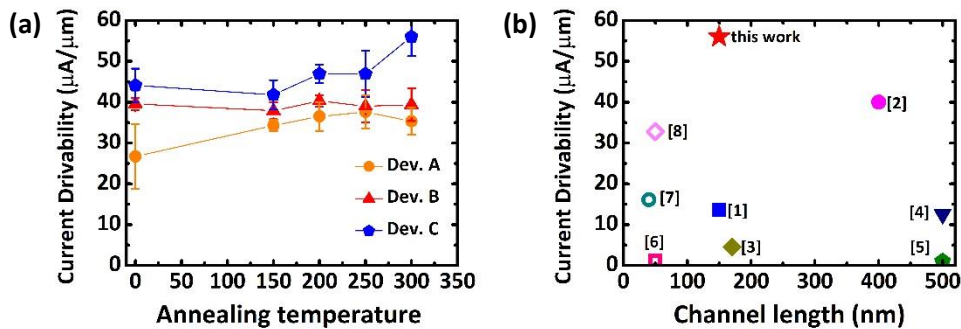


Figure 3. (a) Variations in current drivability of the IGZO VTFTs fabricated with different T_D 's as a function of post-annealing temperature. (b) Bench-mark plot of oxide channel VTFTs in terms of current drivability vs. channel length by means of comparing this work with previous literatures: [1] Nanotechnology, 34, 155301, 2023, [2] IEEE Electron Dev. Lett., 40, 1909, 2022, [3] Electron. Mater. Lett., 18, 294, 2022, [4] Microelectron. Eng., 253, 111676, 2022, [5] SID 2017 digest, 097-9966X, [6] IEDM 21-222, 2021, [7] VLSI Symp. TH2.2, 2020, [8] VLSI Symp. 296, 2022.