ALD Applications
Room Evergreen Ballroom & Foyer - Session AA2-TuP
Microelectronics Poster Session

AA2-TuP-1 Chemically and Mechanically Activated Carbonaceous Materials for Supercapacitor, *D Lam, J Kim,* ***Seung-Mo Lee,*** Korea Institute of Machinery and Materials, South Korea

Carbothermic reduction in the chemistry of metal extraction (MO(s) + C(s) → M(s) + CO(g)) using carbon as a sacrificial agent has been used to smelt metals from diverse oxide ores since ancient times. Here, we paid attention to a new aspect of the carbothermic reduction remained unnoticed till now to prepare activated carbon textile for high rate-performance supercapacitors. On the basis of thermodynamic reducibility of metal oxides reported by Ellingham, we employed not carbon, but metal oxide as a sacrificial agent in order to prepare activated carbon textile. We conformally coated ZnO on bare cotton textile using atomic layer deposition (ALD), followed by pyrolysis at high temperature (C(s) + ZnO(s) → C'(s) + Zn(g) + CO(g)). We figured out that it leads to concurrent carbonization and activation in a chemical as well as mechanical way. Particularly, the combined effects of mechanical buckling and fracture occurred between ZnO and cotton were turned out to play an important role in carbonizing and activating cotton textile, thereby significantly increasing surface area (nearly 10 times) compared with the cotton textile prepared without ZnO. The carbon textiles prepared by carbothermic reduction showed impressive combination properties of high power and energy densities (over 20 times increase) together with high cyclic stability.

AA2-TuP-2 Diamond Field Effect Transistors with Different Gate Lengths of HfO_2 Deposited by Atomic Layer Deposition, ***Changzhi Gu,*** Institute of Physics, Chinese Academy of Sciences, China

The single crystal diamond was treated in hydrogen plasma formed by microwave plasma chemical vapor deposition equipment, and the normally-off hydrogen terminal diamond field effect transistors with different gate lengths were prepared by atomic layer deposition of HfO_2 as gate oxide. We studied the effect of hydrogen treatment time and HfO_2 gate oxide on hydrogen terminal diamond field effect transistor. The experimental results showed that the HfO_2 gate oxide was suitable to fabricate hydrogen terminal diamond field effect transistor and exhibited a normally-off characteristic, which is advantageous for the fabrication of power devices. Furthermore, with increasing the gate length, the drive current density, threshold voltage and transconductance of the diamond device decreased.

AA2-TuP-3 Atomic Layer Deposition of IGZO Thin Films for BEOL Applications, ***Shóna Doyle,*** Tyndall National Institute, Ireland

In the drive for scaling of electronic devices one approach has been the integration of functionality into the back end of line (BEOL). Thin film transitors (TFT) are one such component with high quality devices being realised by PVD indium-gallium-zinc oxide (IGZO). However, the limitations of the PVD deposition process in terms of reliability and coverage in complex 3D topologies is of concern, where uniform sub nanometre films that demonstrate high mobility are required.

Here we have used atomic layer deposition (ALD) to deposit both nano-crystalline/amorphous ZnO and IGZO based laminate structures to generate high mobility thin film materials with sub-nm thickness control. Materials were grown using both thermal and plasma processes on a 200 mm Picosun R200 ALD system. Characterisation, in terms of morphology and composition, were achieved through electron microscopy, x-ray diffraction and x-ray photoelectron spectroscopy. Electrical properties were assessed via 4-point probe and both AC and DC Hall measurements.

AA2-TuP-4 Preparation and Electrical Properties of Polymer-based High-density MIM Capacitors by Plasma-Enhanced Atomic Layer Deposition, *C Fang, M Wang,* ***Chang Liu,*** *D Wu, A Li,* Nanjing University, China

Due to its unique flexibility, efficient and low-cost manufacturing process, and broad application prospects in the information and energy fields, flexible electronic technology has drawn more and more tremendous attentions. Among them, polymer-based high density metal/insulator/metal (MIM) capacitors have triggered a massive amount of research efforts in searching for the most applicable materials and fabrication processing.

In this work, we reported the fabrication and electrical properties of Hf-Ti-O and Hf-Sn-Ti-O MIM capacitors on polymer substrates (PET, PI and epoxy) by plasma-enhanced atomic layer deposition (PEALD). The effect of precursor and cycle ratio on electrical properties of MIM capacitors has been investigated. Organic tetradimethylaminohafnium (TDMAH), inorganic $TiCl_4$ and $SnCl_4$, or tetradimethylaminotitanium (TDMAT) and tetradimethylaminotin (TDMASn) were used as Hf, Ti, Sn metal sources, respectively, with plasma O_2 as O source. The deposition temperature was set to 80~100 °C. By tuning the pulse cycle ratio and cycle number of PEALD, the electrical properties of the Hf-Ti-O and Hf-Sn-Ti-O MIM capacitors were optimized. When the cycle ratio of HfO_2: TiO_2 was 2: 4, the sample of $Hf_{0.82}Ti_{0.23}O_2$ on polymer substrates with total 210 cycles showed larger capacitance density of 7.5 fF/μm² and leakage current density of 1.9×10^{-4} A/cm² at -3 V. When the cycle ratio of HfO_2: SnO_2: TiO_2 was 6: 5: 4, $Hf_{0.81}Sn_{0.06}Ti_{0.18}O_2$ capacitor on polymer substrates with total 300 cycles exhibited better electrical properties of capacitance density of 8.0 fF/μm² and leakage current density of 1.9×10^{-5} A/cm² at -3 V. When the bending radius was no less than 8.2 mm, polymer-based MIM capacitors displayed stable electrical properties without significant change. These results indicate that PEALD Hf-Sn-Ti-O dielectrics on polymers are promising candidate for flexible high-density MIM capacitors application.

AA2-TuP-5 High Voltage MIM Capacitor based on ALD Deposited Crystalline $HfAlO_x$ Film, ***Valentina Korchnoy,*** Technion - Israel Institute of Technology, Israel*; M Lisiansky,* Tower Semiconductor Ltd., Israel*; I Popov, V Uvarov,* The Hebrew University of Jerusalem, Israel*; B Meyler,* Technion - Israel Institute of Technology, Israel

MIM capacitor was developed herein with ALD-fabricated $HfAlO_x$ dielectric layer. MIM capacitor is a key building element in modern CMOS platforms. It may occupy a significant part of the chip area. The high-k dielectric materials were introduced in the advanced production to minimize the footprint area of MIM: HfO_2-based materials grown by ALD replaced conventional dielectrics SiO_2 and Si_3N_4. To prevent the uncontrolled crystallization of amorphous HfO_2 film in a monoclinic phase that degrades its electrical parameters, some dopants (i.e. alumina) are introduced in deposited HfO_2 layer: the composite HfO_2/Al_2O_3 remains amorphous at deposition and during BEOL annealing processes.[1] Thus, amorphous materials are usually used in MIM capacitors located in BEOL. Hafnia doping enhances the composite crystallization (T≥600˚C) into metastable phases of higher symmetry having significantly higher k-value (30-40).[2] Crystalline HfAlOx dielectric has been employed in low voltage capacitors used in DRAM. Some CMOS applications (RF, CIS) require HV MIM capacitor (operating voltage 2.5-3.3V) located as DRAM in IMD0, to benefit from the attractive properties exhibited by crystalline HfAlOx. The increased operational voltage of HV MIM entails thicker dielectric layers compared to those used in DRAM. To take advantage of crystallinity of the HfAlOx film, engineering of the film growth and its crystallization parameters should be optimized for the required film thickness of the HV MIM capacitor. The developed capacitor with EOT≤2nm shows excellent dielectric integrity (V_{BVD}≥8V) along with the low leakage current.

Table 1 presents the plan of experiment where HfO_2-Al_2O_3 laminated stack (12:1) was deposited by ALD in the same run on two types of substrates: Si/SiO2/TiN(70nm) – structure A (MIM) and p-Si/thermal SiO_2(6.4nm) – structure B (MOS). The stack thickness is 14nm. Both pre-deposition (PreDA) and post-deposition (PDA) annealing were performed at the same conditions (T>600˚C). The RTA processing of structure A samples (MIM) was applied in three different flows to distinguish between the effects produced by RTA on the TiN bottom electrode and on the $HfAlO_x$ dielectric layer. Fig.1 shows the scheme of MIM capacitor. The results of electrical characterization are presented in Fig.2 and Table 2. The difference in electrical parameters of MIM capacitors were compared with the detailed structural study of samples 1, 2 and 3 performed by XRD (Fig.3) and TEM/STEM (Fig.5) techniques. Surface characteristics of the TiN electrode was shown in Fig.4. PreDA process allows to prevent the void formation at the TiN/HfAlOx interface and to improve electrical integrity of sample 2.

AA2-TuP-6 Improved Performance of GaN Metal-Oxide-Semiconductor Capacitors byPplasma ALD of AlN Interlayer, ***Dilini Hemakumara,*** *X Li, K Floros, S Cho,* University of Glasgow, UK*; I Guinney, C Humphreys,* University of Cambridge, UK*; I Thayne,* University of Glasgow, UK*; A O'Mahony,* Oxford Instruments Plasma Technology*; H Knoops,* Oxford Instruments Plasma Technology, UK*; D Moran,* University of Glasgow, UK

High quality metal-oxide-semiconductor (MOS) gate stacks with stable threshold voltage are required for future GaN-based power transistors [1]. Here, we report a route to the realization of GaN MOS-capacitors (MOSCAPs) with an ALD AlN interlayer between GaN and Al_2O_3 using a FlexAL ALD system. AlN was grown using plasma enhanced ALD at 300°C

using TMA and N_2 and H_2 plasma. The GaN samples were first exposed to an N_2 150W 5min plasma pre-treatment followed by in-situ ALD of approximately 2nm of AlN. A 20nm Al_2O_3 was then deposited in-situ using thermal ALD at 200^{0}C using TMA and H_2O. The results from these samples were then compared with MOSCAPs that had only an N_2 150W 5min plasma pre-treatment followed by a 20nm thermal ALD Al_2O_3 layer.

20nm Pt/ 200nm Au contacts were deposited ex-situ as the gate contact and the MOSCAPs were measured at room temperature using capacitance-voltage (C-V) and current-voltage (I-V) measurements. The C-V measurements were used to calculate the hysteresis and frequency dispersion of these samples. The hysteresis included the flat band voltage difference between the forward and backward sweep of the C-V curve when swept from -5 to +5V and back to -5V at 1MHz. The frequency dispersion gives the maximum difference in the flat band voltage for C-V curves measured at various frequencies ranging from 1MHz to 1kHz (1MHz, 500kHz, 100kHz, 10kHz and 1kHz).A flat band voltage hysteresis and a frequency dispersion of 200mV was observed for samples that only had an Al_2O_3 gate dielectric while the insertion of an AlN interlayer resulted in a hysteresis and a dispersion of 50mV.

The I-V measurements produced a leakage of 0.016mA/cm^2 at 1V for the sample with only Al_2O_3 while the one with the interlayer produced a leakage of 0.0096 mA/cm^2 at 1V. These positive improvements with the insertion of an AlN interlayer could result due to the prevention of GaO_x sub-oxide formation at the GaN-Al_2O_3 interface [2].

In summary, the insertion of a PE-ALD AlN interlayer between an N_2 plasma treated GaN surface and ALD Al_2O_3 gate dielectric reduces the C-V hysteresis and frequency dispersion by 75% and decreases the leakage current by 40%. Both of these are encouraging for the realisation of high performance GaN power transistors.

1. Fiorenza, P., et al, “Slow and fast traps in metal-oxide-semiconductor capacitors fabricated on recessed AlGaN/GaN heterostructures” . *Appl. Phys. Lett.***106,** 1–5 (2015).

2. Liu, S. *et al.*, “Interface/border trap characterization of Al2O3/AlN/GaN metal-oxide-semiconductor structures with an AlN interfacial layer.”, *Appl. Phys. Lett.***106,** 2–6 (2015).

AA2-TuP-7 2-Dimensional Perovskite Oxide Thin Films Deposited by ALD for High-k Application*, J Ahn,* ***Seung-Won Lee,*** Korea Maritime and Ocean University, Republic of Korea*; C Kim, S Kwon,* Pusan National University, Republic of Korea

As the size of the DRAM is scaled down, the new high-k dielectric materials have received considerable attention. Among high-k materials, the dielectrics based on Zr- and Hf- have extensively been used in semiconductor industry. However, there is a limitation to obtaining an equivalent oxide thickness of under 0.5nm. Therefore, to replace the high-k material based on Zr- or Hf-, new high-k materials, such as rutile-TiO_2 and perovskite oxide, have attracted a candidate in next generation DRAM devices. Meanwhile, 2-D perovskite oxide films made by Langmuir-Blodgett method were reported that the permittivity was measured over 200.[1] However, Langmuir-Blodgett method can’t be applied to electronic applications, especially on the substrate with a high aspect ratio.

Therefore, in this paper, $Sr_xNb_yO_z$ (SNO) thin films with 2-D perovskite structure were deposited on TiN and $SrRuO_3$ substrate using atomic layer deposition (ALD). Then, rapid thermal annealing and laser annealing were performed for crystallization of thin films. Finally, we analyzed physical and electrical properties by RBS, TEM, XRD and semiconductor parameter analyzer.

AA2-TuP-8 High Performance Atomic Layer Deposition (ALD) of Gate Dielectrics for 4H-SiC Power Device Application*, B Lee, M Kang,* North Carolina State University*;* ***Adam Bertuch,*** Veeco-CNT*; V Misra,* North Carolina State University

Silicon carbide is one of most promising substrates for the power Metal Oxide Semiconductor Field Effect Transistor (MOSFET) and other power electronic devices. Due to high density of interface states (D_{it}) at SiO2/SiC interface, the mobility of Si-face (0001) 4H-SiC MOSFETs remains extremely low. Incorporations of nitrogen and phosphorous into the thermal oxide through a high temperature anneal are proven to be effective to suppress the D_{it}. Although the presence of nitrogen or phosphorous improves the mobility, achieved mobility values remain low when compared to the bulk SiC mobility. Additionally, nitrogen and phosphorous incorporations lead to negative threshold voltage (V_T) shift and makes even normally on devices. A positive enough threshold voltage is necessary for safe and reliable operation of power devices. Therefore, to deal with this trade-off between mobility and threshold voltage, deposited dielectrics on 4H-SiC have attracted more research interest to replace the thermal oxide. With deposited gate dielectrics, the substrate consumption is minimized and thus the carbon related defects associated with thermal oxidation can be avoided. Using deposited dielectrics also enables interface engineering to control interface properties independently. Among various deposition method, the atomic layer deposition (ALD) technique has proven to provide good film quality, low substrate damage, precise thickness control, and low temperature processing. This work first evaluates device electrical characteristics and reliability of SiO_2grown by either thermal or plasma ALD. $SiO_2$is the most suitable dielectric due to its large bandgap as well as a high conduction band offset to SiC resulting in suppression of electron tunneling current in SiC MOS devices. It was found that the channel mobility is similar between thermal and plasma ALD SiO_2but thermal ALD oxide shows lower threshold voltage compared to the plasma ALD oxide. Although ALD SiO_2provides positive threshold voltage and good gate insulating property, the SiC/SiO_2interface requires further treatment to enhance the mobility. We have recently demonstrated a novel interface engineering technique to improve the MOSFET mobility by combining ultrathin lanthanum oxide (LaO) at the SiC/dielectric interface and ALD SiO_2. In this study, we deposited ultrathin 1nm LaO followed by 30nm SiO_2using ALD tool without breaking the vacuum. It was found that the channel mobility is enhanced with the incorporation of 1nm LaO between SiC and SiO_2as compared to the device without LaO layer. This combination of ultrathin LaO and SiO_2provides an effective solution to challenges of SiC MOSFETs for power applications.

AA2-TuP-9 Atomic Layer Deposted TiO_2-Based Memristors using In-situ Fabricated Al Doped ZnO Thin Film as Electrodes*, Kai Zhang, P Lin,* Old Dominion University*; A Pradhan,* Advance Material Solution LLC*; H Baumgart,* Old Dominion University

Memristor is a nonlinear and two-terminal passive device, which has ability to change the resistance between high resistive states and low resistive states by applying bias voltage. This property called resistive switching makes the memristors suitable for a wide range of applications in nonvolatile random access memory, dynamic random access memory and flash memory. In recent years, Metal-oxide based memory devices have drawn significant attention due to their high-density integration, high endurance, fast switching behavior, low power consumption and simple structure. In addition, among the promising binary transition metal oxide materials, such as nickel oxide, zirconium oxide, zinc oxide, hafnium oxide, and titanium oxide, TiO_2 films are extensively used to fabricate the nonvolatile memristor devices due to its simple structure and compatible with CMOS integration process. Recently, ZnO has been widely used for various applications due to its good electrical conductivity, wide band gape (3.37 eV), high exciton binding energy (~60 meV), low cost, nontoxicity, high mechanical and thermal stability. When doped with Aluminum ZnO grown via atomic layer deposition (ALD) has been reported to show resistivity values ranging from insulating to on the order of 10^{-3} Ω·cm, which is suitable for memory device electrodes.

Currently, the most common methods used were magnetron sputtering, pulsed laser deposition, thermal oxidation, electrodeposition, chemical vapor deposition, sol gel chemical reaction, and atomic layer deposition. The ALD is a self-limiting technique that allows atomic layer growth each time. ALD can precisely control the film layer thickness, stoichiometry, composition, uniformity, and sharp interface. ALD also shows perfect conformal coverage when it deposits thin film on complex surface structures. Therefore, ALD is considered as a novel and competitive method to deposit MIM memory structures. To create such devices, transparent Al:ZnO film was grown on Si wafers as an transparent electrode followed by an active layer of TiO_2 film, then the other layer of Al:ZnO was deposited *in-situ* on the TiO_2 layer to form memristor structures. All the thin films in the structures were synthesized by the ALD system sequentially.

Several physical characterization techniques have been employed to determine the ALD films of memory devices. The crystal structure was analyzed by X-ray diffraction. The film morphology was determined by field emission scanning electron microscopy. The surface roughness was analyzed by atomic force microscopy. The electric properties were measured by semiconductor analyzer. The results demonstrate a fairly good memristive device.

AA2-TuP-10 Homogeneously Doped Atomic Layer Deposition Zinc Tin Oxide Thin Films for Improving Contact Resistance in Semiconductor Device Applications, ***Alex Ma,*** University of Alberta, Canada*; T Muneshwar,* Synthergy Inc., Canada*; D Barlage, K Cadien,* University of Alberta, Canada

For thin film semiconductor device applications, the formation of high quality contacts is critical. Currently, it is difficult to realize ohmic contacts on zinc oxide (ZnO) thin films especially for applications that require more resistive active layers e.g. thin film transistors (TFTs) and Schottky diodes. In this work, we investigate the contact resistance in thin film devices that employ ZnO active layers grown by low temperature plasma-enhanced atomic layer deposition (ALD) with the gated transmission length method (TLM). The contact performance in intrinsic ZnO devices are compared to identical devices but with a homogeneously doped ALD zinc tin oxide (ZTO) interlayer inserted between the semiconductor body and metal contact. By incorporating a small percentage of tin (Sn) in the ZnO during ALD growth, we observed an increase in the film's electron concentration resulting in lowered contact resistance.

AA2-TuP-11 AlGaN/GaN Layers Obtained by Atomic Layer Deposition Targeting Thin Film HEMT, ***Joaquin Alvarado,*** *M Chávez,* Benemérita Universidad Autónoma de Puebla, Mexico*; S Gallardo,* CINVESTAV-IPN, Mexico*; Y Sheng, D Muenstermann,* Lancaster University, UK

$Al_xGa_{1-x}N$ and GaN films were obtained using Plasma enhanced Atomic Layer Deposition (PE-ALD) at 300 °C, we study the effect of Al content variation on the optical and structural and electrical performance. XRD measurements show the hexagonal structure, SIMS profile signals reveals the main components of $Al_xGa_{1-x}N$.

Experimental

AlGaN thin films were deposited on silicon wafers via atomic layer deposition using a mega cycle which consists of sub cycles of AlN and GaN to obtain the $Al_xGa_{1-x}N$ alloy. The AlN sub cycle consist of (1) pulse of Trimethyl Alluminium (TMA), (2) Ar purge, (3) H_2/N_2 plasma and (4) Ar purge, the growth ratio is (0.5Å/cycle) at 300°C, the total number of megacycles were 215. GaN sub cycles consist of (1) pulse of Trimethyl Galliu (TMGa), (2) Ar purge, (3) H_2/N_2 plasma and (4) Ar purge, the growth ratio is (0.2Å/cycle) at 300 °C, the total number of megacycles were 131. The number of megacycles were calculated in order to obtain ~20 nm.

Results

The XRD patterns of $Al_xGa_{1-x}N$ on silicon substrates growth with 0.3 and 0.6 Al content were performed. Two peaks were observed in the sample $Al_{0.3}Ga_{0.7}N$ the peak located at 2θ=34.5° (002) is assigned to hexagonal phase of GaN and a second peak at 2θ=32.3° (100) correspond to the hexagonal phase of AlN. The sample $Al_{0.6}Ga_{0.4}N$ show peaks at 2θ=32.3° , 34.3° ,37.0° assigned (100), (002), (100) AlN. Furthermore, from photoluminescence characterizations it is possible to observe in the $Al_{0.3}Ga_{0.7}N$ sample a yellow luminescence band situated at 2.32 eV, which is related to Gallium and N vacancies, carbon defects, as well as to the high concentrations carriers 10^{19} cm^{-3} [1]. The peak observed at 2.2 eV is associated to dislocations defects [2]. However, a sample which contains higher content of Al didn't show PL signal.

On the other hand, by SIMS sputtering time profile it is possible to observed that the sample with $Al_{0.3}Ga_{0.7}N$ show a non-uniform Al content, although $Al_{0.6}Ga_{0.4}N$ show a better Al distribution film. Electrical characterizations of the deposited films will be also included.

AA2-TuP-12 High-Temperature Thermal Stability of ALD-TiN Metal Gate on *In-situ* Al_2O_3/Y_2O_3/(In)GaAs(001): Toward the Self-Aligned Gate-First Process, ***Lawrence Boyu Young,*** *H Wan, J Huang, K Lin, J Liu, Y Lin,* National Taiwan University, Republic of China*; J Kwo,* National Tsing Hua University, Republic of China*; M Hong,* National Taiwan University, Republic of China

High-k metal gate (HKMG) technology has been introduced since the 45-nm node complementary metal oxide semiconductor (CMOS). The gate-first process was replaced by the gate-last process because of the threshold voltage pinning caused by the subsequent high-temperature process[1]. The gate-first process provides a capability to reduce the process complexity, and is more economic than the gate-last process. To realize high-performance MOS field-effect transistors (MOSFETs) using self-aligned gate-first process, the thermal stability of MOS structure must be excellent to sustain the subsequent high temperature process. With the higher electron mobility, GaAs-based III-V semiconductors have potential to replace the current Si-based CMOS technologies. However, the reported thermal stability between high-k/III-V was limited to 500~600°C caused by the inter-diffusion. In our previous study, ultra-high thermal stability above 850°C between in-situ grown oxide/III-V interface was attained[2,3], critical for the present study of atomic layer deposition (ALD)-TiN/oxide/(In)GaAs thermal stability at temperatures ranging from 850 to 950°C. Here, we have studied the samples with different post-metallization annealing (PMA) using transmission electron microscopy (TEM), J-E, and C-V characteristics of the MOS capacitors (MOSCAPs). The samples were prepared in a ultra-high vacuum (UHV) multi-chamber growth/analysis system (Fig. 1). The detailed fabrication process and the schematic structure of the MOSCAPs are shown in Fig. 2 . The TEM shows the smoothness in an atomic scale of the ALD-TiN/high-k/(In)GaAs interfaces. The interface remained intact without degradation after 800°C 5s in He ambient (Fig. 3). From the J-E curves (Fig. 4), the leakage current densities of the MOSCAP with different PMA in N_2 show no degradation after 900°C annealing for 10s. The leakage current density of the MOSCAPs maintained below 10^{-7} A/cm² at electric fields of ± 4 MV/cm, which is the same with that of the MOSCAP without PMA. A different behavior was found in the MOSCAP with PMA in He. The leakage current density raised sharply in the negative bias region, probably resulted from the generation of nitrogen vacancies during the high temperature annealing in He. Similar features were found in the C-V characteristics (Fig. 5). With the PMA in N_2, the C-Vs showed no degradation after 900-950°C annealing, while the MOSCAP was too leaky to measure the C-Vs for the MOSCAP with PMA in He with temperatures above 900°C. The excellent electrical and thermal stability of the MOS structures with TiN gate are vital to realize high performance GaAs inversion channel MOSFETs using a gate-first process.

AA2-TuP-13 Identification of Interfacial Defect in ALD Grown Al_2O_3/GeO_x/Ge Gate Stack, ***Jinjuan Xiang,*** *L Zhou, X Wang, X Ma, T Li, W Wang,* Institute of Microelectronics of Chinese Academy of Sciences, China

Germanium (Ge) has attracted tremendous interest as a channel material for high performance complementary metal-oxide-semiconductor (CMOS) devices. The interfacial cfixed charges are detrimental to the performance promotion of Ge MOSFET devices as they can form Coulomb scattering center to reduce channel carrier mobility and device reliability. Thus we experimentally investigate the interfacial defect in the GeO_x/Al_2O_3 gate stack grwon by ALD using X-ray photoelectron spectroscope (XPS) and electrical charateristics by capacitance-voltage (*C-V*) measurement. For GeO_x interlayer by ozone oxidation, oxygen vacancies exist and show positive charges at the Ge/GeO interface. The O_2 annealing is helpful to decrease the oxygen vacancy defect. For the GeO_x/Al_2O_3 interface, oxygen dangling bonds exist, and show negative charges. This work can be effectively applied to engineer the interface promotion and enhance the performance of Ge-based devices.

AA2-TuP-14 Modifications of the Electrical Properties of MOS Capacitors Based on Bilayer Gate Metallization - WC_xN_y Capped by CVD Molybdenum on SiO_2 and on ALD Al_2O_3, ***Ekaterina Zoubenko,*** Technion - Israel Institute of Technology, Israel*; I Fisher, S Thombare, P Van-Cleemput, M Danek,* Lam Research Corp.*; M Eizenberg,* Technion - Israel Institute of Technology, Israel

Refractory metal nitrides and carbides, deposited by ALD, are attractive for gate metallization of 3D metal-oxide-semiconductor (MOS) devices, due to the good thermal and chemical stability and metal effective work function (EWF) variation capability. However, obtaining low resistivity of the gate metallization is challenging. Therefore, a bilayer approach, where a thin refractory metal carbide/nitride liner capped by a pure metal, is implemented. The liner determines the EWF and serves as a nucleation layer and a diffusion barrier for the contact metal. Currently, Tungsten is commonly used as a local interconnect conductor. Due to its resistivity and device performance challenges, Molybdenum is considered as an alternative capping layer.

The objective of the current research is to investigate the structural and the electrical properties of a bilayer metallization: thermal-ALD tungsten carbo-nitride, WCN (WC_xN_y), liner with thicknesses of 10/20/30Å covered by 100Å CVD-Mo cap. The evolution of the properties upon annealing at 750°C in forming gas (FG -10%H_2, 90%Ar) and vacuum (10^{-6}torr) is correlated with the values of the EWF on thermal SiO_2 and on ALD Al_2O_3/SiO_2. The metal stack structure and composition were studied by XRD, STEM-EDS, and ToF-SIMS. The sheet resistance was measured by the four-point probe technique. The EWF of the WCN/1kÅ Mo metal stack on SiO_2 and on Al_2O_3 was studied using capacitance-voltage measurements of MOS devices by plotting the flat-band voltage versus the effective oxide thickness.

It was found that the lowest sheet resistance of as-deposited samples was obtained for the metal stack on the 10Å WCN liner (26Ω/□); annealing at FG led to sheet resistance decrease up to 11Ω/□. The EWF of the as-

deposited samples is determined by the WCN layer: a value of 4.8eV on SiO_2, as was obtained by a 30Å WCN/W reference sample, and a value of 5.35eV on Al_2O_3/SiO_2, demonstrating a difference of ~0.4eV attributed to a dipole at the Al_2O_3 /SiO_2 interface, earlier obtained in our group. Both thermal treatments induced Mo diffusion towards the interface with the dielectric, but the annealing ambient effect on metal crystallinity and Mo diffusion rate is different. Annealing at vacuum caused grain growth of the cubic W_2N phase and stabilization of the EWF to a value of 4.8eV on SiO_2. FG annealing led to BCC-Mo grain growth, significant Mo diffusion towards the interface, and EWF on SiO_2 decrease of 0.2eV. Similar EWF decrease due to FG annealing was observed on Al_2O_3. This, combined with the low resistivity, makes WCN/Mo stack a good candidate for many applications, e.g. FDSOI devices.

AA2-TuP-15 Effect of Metal-insulator Interface on Dielectric Properties of Ultrathin Al_2O_3 and MgO Fabricated using *In-situ* Sputtering and Atomic Layer Deposition, ***Jagaran Acharya**, J Wilt, R Goul, B Liu, J Wu,* The University of Kansas

We have investigated the properties of ultrathin $Al_2O_3$and MgO in metal-insulator-metal (M-I-M) trilayers fabricated using *in situ* integrated sputtering and atomic layer deposition (ALD). The quality of ultrathin Al_2O_3 was found to be significantly dependent on the pre-ALD conditions which lead to extremely different M-I interface. After optimization of ALD processing parameters, M-I interfacial layer (IL) was reduced to a negligible level obtaining a dielectric constant (ε_r) up to 8.9 on the Al_2O_3films in a thickness range between 3.3-4.4 nm, corresponding to an effective oxide thickness (EOT)~1.4-1.9 nm respectively comparable to high-K dielectrics. While ε_r decreases at a smaller Al_2O_3 thickness, the hard-type dielectric breakdown 32 MV/cm and in situ scanning tunneling spectroscopy (STS) revealed band gap ~2.63 eV confirming high quality dielectric as good as an epitaxial Al_2O_3 film. This result suggests that the IL is unlikely a dominant reason for the reduced ε_r at the Al_2O_3 thickness of 1.1-2.2 nm and is due to electron tunneling as supported by transport current-voltage measurement. However, non-optimal conditions result in the growth of significant IL with drastically reduced ε_r~0.5-3.3. The properties of MgO with and without 5C-ALD Al_2O_3 studied in the thickness range 2.5-5 nm point out significance of seed layer in fabrication of high-quality dielectrics, approaching ε_r~9 for 5C-ALD-Al_2O_3/ALD-MgO at thickness 3.8-4.9 nm corresponding to EOT~1.6-2.1 nm respectively. But, 40C-ALD MgO without seed layer has unexpectedly lower ε_r~3-4 possibly due to poor nucleation forming an interfacial layer, and correspondingly increase in the leakage current. The similar decreasing trend in ε_r with decrease in MgO thickness is observed but at thickness greater than that of Al_2O_3, due to higher leakage current observed for MgO dielectrics and also confirmed by in situ STS analysis. Our results demonstrate the significance of controlling the nucleation in ALD to achieve better M-I interface in order to fulfill the demand for leak-free and defect-free high-quality ultrathin dielectrics an alternative for low-cost gate dielectric for CMOS, and tunnel junction for quantum computing and memory applications.

AA2-TuP-16 Thermal and Plasma ALD Al_2O_3 Gate Insulator for GaN Electronic Devices Characterized by CV-Stress Measurements, ***Nicole Bickel**, E Bahat Treidel, I Ostermay, O Hilt, O Krüger,* Ferdinand-Braun-Institut, Germany*; F Naumann, H Gargouri,* SENTECH Instruments GmbH, Germany*; J Würfl, G Tränkle,* Ferdinand-Braun-Institut, Germany

The technology of atomic layer deposited (ALD) Al_2O_3 films is ideally suited for fabrication of high quality GaN MISFET's gate insulator especially in vertical GaN n-channel transistor technology (Fig. 1). The gate oxide technology is a very crucial process step as it influences transistor functionality such as normally-OFF operation, hysteresis and low positive threshold voltage drift. Furthermore, dependent on the transistor design the gate oxide/channel interface may also determine ON-OFF-ratio. For qualifying and characterizing the gate insulator film technology, circular-planar MIS-capacitors were formed on a *n*-GaN layer (Fig. 2). The 25 nm thick Al_2O_3 films were deposited by plasma enhanced atomic layer deposition (PEALD) and thermal atomic layer deposition (ThALD) in SENTECH ALD system SI PEALD. Different in-situ surface pre-treatment conditions such as NH_3-plasma, NH_3-flow and without any pre-treatment were tested to optimize the GaN/Al_2O_3 interface. After top electrode metallization the capacitors were annealed at 350°C in N_2-ambient to achieve a large $\Delta C_{ON\text{-}OFF}$. Accumulated capacitance-voltage-(CV)-scans were performed to evaluate the insulator charging effects, to identify possible shifts in the CV-profile and to gain insight into bulk and interface charging phenomena (see Figs. 3 and 4). While measuring the accumulated bidirectional scans the maximum positive stress bias voltage was increased in 2 V steps from 0 V to 16 V after each bias sweep. The capacitance was measured at 1 MHz and 1 V AC amplitude. According to Figs. 3 and 4 a negative bias down to -15 V has turned out to be sufficient to empty the interface traps. PEALD and NH_3-plasma treated samples show a significant broadening of the positive bias stress CV-profile. Furthermore the flat band voltage shifts up to 7.2 V (Fig. 5). In contrast, the ThALD films with NH_3-plasma pre-treatment show a reduced broadening with a flat band voltage shift of only 2.9 V. When using NH_3-plasma pre-treatment, the calculated maximum negative fixed-oxide charges are less for ThALD ($-\Delta N_{OX}$ 5.1×10^{12} cm^{-2}) as compared to PEALD ($-\Delta N_{OX}$ 1.1×10^{13} cm^{-2}), see Fig. 6. Therefore thermal ALD in combination with NH_3-plasma pre-treatment is very suitable for GaN MISFET technology.

AA2-TuP-17 Variable Morphology Highly-Conformal Diffusion Barriers for Advanced Memory and Logic Applications, ***Hae Young Kim**, S Rathi, B Nie, N Naghibolashrafi, Y Okuyama, S Chugh, J Heo, S Jung, J Mack, N Mukherjee,* Eugenus, Inc.

Atomic layer deposition (ALD) of metallic ternary TiSiN films is associated with a variety of morphological and structural variations. Among these phenomena are the thickness and stoichiometric-dependent amorphous to crystalline phase transitions, film density changes, surface roughness and film resistivity variations. In the case of TiSiN films deposited via thermal ALD at temperatures of about T<600° C, using chlorine-based Si precursors, titanium tetrachloride and ammonia, the film structure is highly dependent on the total Si incorporated in the film. In this work, we demonstrate the tunability of crystalline phase in highly conformal TiSiN films with varied Si content. TiSiN films were deposited on high aspect ratio structures using a Eugenus 300mm commercial QXP mini-batch system. Film thickness and Si content were varied, and corresponding structural analysis was performed using multiple characterization techniques. X-ray diffraction and reflectivity studies of these films showed a reduction in film density and transition from nano-crystalline to pure amorphous phase with increase in Si fraction. Cross-section high resolution transmission electron microscopy (HRTEM) and selected area electron diffraction (SAED) pattern analyses corroborates with the X-ray analysis that high-Si TiSiN films exhibit a fully amorphous structure. Moreover, control of Si fraction in the film enables tuning of the morphology from polycrystalline to fully amorphous; in all cases, excellent step coverage on high aspect ratio structures were obtained.

AA2-TuP-18 Room Temperature Deposition of Hafnium Oxide by Atomic Layer Deposition for Gating Applications, ***Pragya Shekhar**, S Shamim, S Hartinger, J Kleinlein, R Schlereth, H Buhmann, L Molenkamp,* University of Wuerzburg, Germany

The advancement of fabrication techniques for nanostructures devices has led to technological breakthrough in semiconductor industries. Apart from the lithographic developments, high-κ materials like ZrO_2 and HfO_2 have been employed as gate dielectric for efficient control of the carrier density. In this regard, atomic layer deposition (ALD) has been used to grow these insulators as it produces highly uniform and conformal layer with precise thickness. Previous works to grow HfO_2 by ALD require higher temperature (>100 ^oC) for microelectronic devices has been done. However, many devices and materials have additional constraints that their properties degrade at higher temperatures. This limits the operating temperature at which the various fabrication processes can be carried out. For our research in the field of topological physics, mercury telluride (HgTe) topological insulators (Tis) are significant due to its versatility and tunability from trivial to 2D TI to 3D TI to Weyl by tuning the thickness and applied strain (compressive or tensile). However, the transport properties degrade when the HgTe wafer are heated above 80 ^oC . To overcome this problem, we have developed a room temperature ALD process for growing HfO_2. A comprehensive study of structural and transport properties of devices containing HfO_2 gate dielectrics was carried out and results has been compared to device containing coventional SiO_2/ Si_3N_4 multilayers insulator films grown by plasma enhanced chemical vapour deposition (PECVD).This comparison demonstrates that our ALD grown insulator is superior in terms of structural properties. We have already shown that microstructures fabricated with ALD grown insulator shows quantum spin hall effect for 2D HgTe based devices. This capability is critical for understanding the properties of microscopic devices and may provide new insights in the field topological insulators. Our process is not just limited to HgTe (e.g. we use Si for process control) but can be easily adapted to other material systems which also require low temperature lithography process in order to retain the intrinsic property of material.

AA2-TuP-19 Influence of Surface Cleaning Process on Initial Growth of ALD-Al_2O_3 and Electrical Properties of Pt/Al_2O_3/β-Ga_2O_3 MOS Capacitors, ***Masafumi Hirose***, Shibaura Institute of Technology, Japan; *T Nabatame,* National Institute for Materials Science, Japan; *E Maeda,* Shibaura Institute of Technology, Japan; *A Ohi, N Ikeda, Y Irokawa, Y Koide,* National Institute for Materials Science, Japan; *H Kiyono,* Shibaura Institute of Technology, Japan

β-Ga_2O_3 power device with metal-oxide-semiconductor (MOS) structure have been widely investigated. Al_2O_3 is the leading candidate as gate insulator because of relatively stable amorphous structure, a high dielectric constant (k) of 8 - 9 and a large bandgap of 6.5 - 6.8 eV. Al_2O_3 films are generally formed by atomic layer deposition (ALD). However, it remains big issues such as an abnormal flatband voltage (V_{fb}) shift and a large interface state density (D_{it}). To improve these electrical properties, various surface cleaning techniques of the substrate have been considered. In this study, we investigate how the surface cleaning technique affects to morphology of the surface of β-Ga_2O_3 and electrical properties of Pt/Al_2O_3/β-Ga_2O_3 MOS capacitors.

At first, n-β-Ga_2O_3 epilayer (2.0×10^{16} cm^{-3}) / n^+-β-Ga_2O_3 (3.7×10^{18} cm^{-3}) substrates (n-β-Ga_2O_3) were cleaned under four conditions: just a SPM for 5min, and SPM for 5 min (SPM), followed by BHF for 1 (BHF1), 10 (BHF10), and 30 min (BHF30). 25-nm-thick Al_2O_3 films were deposited on n-β-Ga_2O_3 substrates by ALD at 300 °C using TMA precursor and H_2O gas. Finally, Pt gate electrodes and Ti/Pt ohmic electrode were deposited.

The minimum root mean square (RMS) value (0.36 nm) of the n-β-Ga_2O_3 substrate was observed after SPM treatment. The RMS values (~ 0.6 nm) increased drastically when BHF treatment carried out even for 1 min and the value was unchanged even if treatment time was longer. In addition, the n-β-Ga_2O_3 substrate was etched by 0.9 nm for the BHF30. This is because the increase of the surface roughness is due to the heterogeneous etching of the n-β-Ga_2O_3 substrate. The Al_{2p} XPS intensities of the Al_2O_3 films after ALD 5 cycles for the BHF10 and BHF30 decreased by about 25 % compared to the SPM and BHF1, suggesting that the surface roughness affects to the initial growth of the Al_2O_3.

The MOS capacitor exhibited similar *J-V* properties regardless of the surface treatment techniques, indicating that the characteristic of the Al_2O_3 films was unchanged. On the other hand, the V_{fb} hysteresis ($V_{fb\ hys}$) due to the trapped/detrapped electrons increased as the BHF treatment time increases. The D_{it} energy distribution due to the fixed charge, which was calculated using conductance method, increased with increasing the BHF treatment time. These $V_{fb\ hys}$ and D_{it} behaviors are in good agreement with the data of the surface roughness of the n-β-Ga_2O_3 substrate. Considering to these data, note that the fixed charge and trapped/detrapped electrons occur at the Al_2O_3/n-type β-Ga_2O_3 interface. Therefore, the BHF surface treatment technique is not necessary promising from the viewpoint of the interface characteristics.

AA2-TuP-20 Reliable Gate Stack Development Employing Plasma Assisted Atomic Layer Deposited HfO_xN_y on InGaAs Substrate, ***Sukeun Eom***, *M Kong, K Seo,* Seoul National University, Republic of Korea

We developed an advanced plasma-assisted atomic-layer-deposited (PA-ALD) HfO_xN_y process targeted on InGaAs substrate. The developed ALD process is consisted of isopropyl oxidant precursor and in-situ cyclic N2 plasma nitridation that improves both interface and dielectric bulk quality as well. The interface chemistry and capacitance-voltage characteristics of HfO_xN_y / InGaAs MOS devices are investigated. Clear oxide related elements were eliminated using our ALD process confirmed by XPS and STEM measurements. The IPA-based HfO_xN_y/n-$In_{0.53}Ga_{0.47}As$ MOS capacitor exhibited a significant decrease of interface trap density, D_{it}, of 4.5×10^{11} $eV^{-1}cm^{-2}$ at E_c - E_t = 0.3 eV and outstanding inversion behaviors. Morevover, substantial improvement was found not only in n-type substrates but also in p-type substrates as well. The significant mid-gap D_{it} decrease is responsiblefor this inversion behavior. The improvement mechanism of the proposed technology is assumed to be that nitrogen incorporation reduces oxygen vacancies which act as oxygen diffusion paths and with the use of IPA oxidant the interface would be strongly protected during pre- and post-dielectric deposition. Detailed electrical characteristics such as positive-bias-temperature-instabiltiy characteristics were investigated.

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