Tuesday Morning, July 23, 2019

Atomic Layer Etching
Room Regency Ballroom A-C - Session ALE2-TuM
Alternative Methods to ALE

Moderators: Jean-François de Marneffe, IMEC, Satoshi Hamaguchi, Osaka University, Japan

10:45am **ALE2-TuM-12 Atomic Layer Etching for Germanium using Halogen Neutral Beam =Comparison between Br and Cl Chemistry=***, T Fujii,* ***Daisuke Ohori,*** Tohoku University, Japan*; S Noda,* National Institute of Advanced Industrial Science and Technology, Japan*; Y Tanimoto, D Sato, H Kurihara,* Showa Denko K.k.*; W Mizubayashi, K Endo,* National Institute of Advanced Industrial Science and Technology, Japan*; Y Li,* National Chiao Tung University*; Y Lee,* National Nano Device Laboratories*; T Ozaki, S Samukawa,* Tohoku University, Japan

Recently, 3D Fin field-effect transistors (FETs) have been developed for breaking through limitations of the short-channel effect for highly scaled metal-oxide-semiconductor (MOS) FETs. However, the Ge channel formation for Fin FET has not been deeply investigated since the Ge etching reaction is not known well compared to the Si etching reaction. As a result, the carrier mobility degradation was observed by electron scattering due to surface roughness and defects on the channel sidewall surface etched by conventional plasma etching (PE). In the PE, energetic ion bombardment and ultraviolet (UV) light irradiation cause a large side-etching, sidewall surface defects, and sidewall surface roughness. These lead to the degradation of carrier mobility and I-V characteristics [1]. To realize higher performance electrical characteristics without compromising the intrinsic high carrier mobility of Ge, atomic layer defect-free, roughness-free, and profile-controlled etching must be accomplished for future sub-10 nm Ge Fin FET. In this work, we demonstrated atomically flat, extremely high selective and defect-free etching with the hydrogen bromide (HBr) neutral beam etching, and investigated the mechanism compared with the Cl_2 NBE.

We investigated Ge etching rate dependence on the substrate temperature from -20 to 150 ºC by using HBr and Cl_2 neutral beam. Sample structure was p-type Ge (100) wafer with SiO_2 line pattern mask of 150 nm in width of a nanoimprint.

We carried out the cross-sectional SEM observation and ellipsometer measurement for checking the Ge etching rate and SiO_2 etching rate, respectively. For the HBr NBE, the Ge etching rate was almost constant at 35 nm/min from -20 to 90 ºC. On the other hand, for the Cl_2 NBE, the Ge etching rate linearly increased from 38 to 45 nm/min from -20 to 150 ºC. SiO_2 etching rate for HBr and Cl_2 NBE were 0.3 nm/min and 2.8 nm/min at any substrate temperature, respectively. The HBr NBE could realize almost 10 times higher etching selectivity as compared with Cl_2 NBE. Moreover, the sidewall etching for HBr NBE was perfectly eliminated from -20 to 90 ºC. In contrast, the sidewall etching for Cl_2 NBE occurred at more than 90 ºC. It is considered that non-volatile Bromide protected layer, such as $GeBr_4$ and $Si_xBr_yO_z$ was formed on the Ge sidewall and SiO_2 top surface in case of using HBr. HBr NBE could perfectly eliminate the sidewall etching and obtain extremely high etching selectivity to SiO_2 even at more than 90 ºC . In conclusion, we succeeded to fabricate the Ge Fin structure of highly anisotropic and extremely high selectivity with HBr NBE.

[1] W. Mizubayashi, et al., Appl. Phys. Express, 10, 026501 (2017).

11:15am **ALE2-TuM-14 A New Etching / Passivation Process in Cyclic Mode for Spacer Etching in 3D CMOS Integrations***, O Pollet,* CEA-LETI, France*; N Posseme,* Univ. Grenoble Alpes, CEA, LETI, France*; V Ah-Leung,* ***Valentin Bacquie,*** CEA-LETI, France

With ever-decreasing gate length in CMOS technology, integrations have changed from planar to 3D architectures, such as FinFET or stacked nanowires, where the channel is a tall and narrow structure protruding from the surface, thereby providing a better electrostatic control and reduced leakage. However from an etch standpoint this raises new challenges particularly for spacer formation since the stopping layer has become a structured surface instead of being flat, which induces the formation of parasitic spacers on channel sidewalls. To overcome this issue overetch must be significatively lengthened, from 30-50% in planar CMOS to 200-300% in 3D CMOS. Considering other requirements such as no CD loss, no channel material loss or damaging, spacer etching has turned into a very challenging process.

Conventional processes based on fluorocarbon chemistries like $CH_3F/CH_4/O_2$ do not provide sufficient selectivity to silicon to enable long overetch required to get rid of spacers on channel sidewalls without considerably consuming or damaging the channel material. To improve selectivity a new process was proposed recently, that contains $SiCl_4$ in addition to fluorocarbon in the etching chemistry.

XPS analyses showed that this specific gas composition leads to the deposition of SiO_xF_y, which acts as a passivation layer on silicon, instead of the usual carbon-rich organic film deposited with CH_zF_w/O_2 chemistries. Ellipsometry measurements highlighted that SiO_xF_y passivation grows preferentially on silicon than on silicon nitride, which allows etching to carry on this material while silicon is passivated. Less than 1nm of silicon consumption is consistently measured even for long process times while at the same time silicon nitride is etched linearly providing a selectivity up to 40:1 between nitride and silicon.

To further improve process performance this $SiCl_4$-containing process was combined in a cyclic mode with a non-selective CHF_3 step. The $SiCl_4$ step function is to etch silicon nitride while depositing passivation on silicon. During the CHF_3 step both silicon nitride and passivation on silicon are etched and respective step times were set up in such way that silicon nitride is linearly etched at a rate of 7.3nm/cycle while the silicon surface is permanently covered by the SiO_xF_y layer. This ALE-inspired process was demonstrated on a stacked nanowires integration: a 12.5nm thick SiN IRAD spacer was etched with very limited CD bias on the gate while parasitic spacers formed on 36nm high active area sidewalls were thoroughly removed without inducing more than 1.5nm silicon consumption.

11:30am **ALE2-TuM-15 Atomic Layer Etching of Transition Metals with Gas Cluster Ion Beam Irradiation and Acetylacetone***,* ***Noriaki Toyoda,*** *K Uematsu,* University of Hyogo, Japan

Atomic layer etchings (ALE) of transition metals with gas cluster ion beam (GCIB) and acetylacetone were investigated. In general, the ion energy in the removal step in ALE is several tens of eV, which is higher than the sublimation energy of the surface layer (several eV). These excess energies might be the origin of the damages on the target materials. We have investigated the feasibility of GCIB as energetic ions in the removal steps of ALE process. Since GCIBs are aggregates of thousands of gas atoms or molecules, the energy/atoms or energy/molecules can be easily reduced to several eV even though the total energy of GCIB is several keV. In additions, since GCIB induce dense energy deposition without severe damage, the bombarded area experiences transient high-temperature and high-pressure conditions. As a result, chemical reactions are enhanced at low-temperature. In the previous study, ALE of Cu films was demonstrated successfully using O_2-GCIB and acetic acid.

In this study, we have investigated ALE process for transition metals (Cu and Ni) using acetylacetone. We separated each etching step as following; (1) adsorption of acetylacetone on metal oxide, (2) evacuation of residual acetylacetone vapor, (3) irradiation of O_2-GCIB to remove metal oxide. Effects of the following etching parameters on ALE were investigated from real-time thickness on a quartz crystal monitor; acceleration voltage of oxygen GCIB, irradiation time of GCIB, exposure time of acetylacetone.

When the acceleration voltage of O_2-GCIB is 20 kV, very thin layer of nickel oxide with adsorbed acetylacetone is removed quickly, however, Ni atoms are physically sputtered. Consequently, the etching process with 20 kV oxygen GCIB is not self-limiting. On the contrary, surface nickel oxide with adsorbed acetylacetone are removed by 5 kV O_2-GCIB and there is no physical sputtering. Since the average cluster size of O_2-GCIB is 3000 molecules/ion, the energy/molecule is below 2 eV. By using 5 kV O_2-GCIB, self-limiting removal step is realized.

11:45am **ALE2-TuM-16 Atomic Layer Etching at Atmospheric Pressure***,* ***Eugen Shkura****, D Theirich, K Brinkmann, T Haeger,* University of Wuppertal, Germany*; J Schneidewind, M Siebert,* SENTECH Instruments GmbH, Germany*; T Riedl,* University of Wuppertal, Germany

Atomic Layer Etching (ALE) is a cyclic process which is based on sequential surface reaction of two or more reactants and ideally provides control on the monolayer level. In the last decade the main focus was on two types of ALE. The first approach relies on the chlorination and sometimes fluorination to initially create metal-halide species at the surface which are subsequently removed by a plasma [1,2]. Another approach is thermally driven ALE, e.g. by using HF and $Sn(acac)_2$ to etch metal oxides [3]. More recent reports indicated isotropic etching by using radically driven, plasma enhanced ALE [4]. In all these examples, the ALE process is vacuum based and as such provides some limitations towards high throughput and low manufacturing costs. Here, we introduce a novel process for Atomic Layer Etching at atmospheric pressure (AP-ALE). As a case study, we investigate the etching of ZnO by AP-ALE and spatial AP plasma enhanced-ALE by using

Hacac at substrate temperatures in the range of 80-140 °C. Ozone as well as an atmospheric pressure dielectric Ar/O_2 barrier discharge is used for AP-ALE and spatial AP Plasma Enhanced-ALE, respectively. In-situ quartz crystal microbalance as well as ex-situ spectroscopic ellipsometry were used to characterize the etching process. Depending on the processing conditions, an etch per cycle of 0.5 to 5 Å is found. Ex-situ AFM measurements before and after ALE show a modification of ZnO-Surface and a decrease in film thickness. Furthermore, growth characteristics in dependence of process parameters like substrate velocity and substrate temperature were investigated. We discuss the prospects to use spatial AP-ALE for materials other than metal oxides, such as III-V semiconductors like GaN or AlGaN.

[1] K.J. Kanarik et al. Solid State Technology 56(8) 14-17 (2013).

[2] S. Rauf et al. J. Appl. Phys. 101, 033308 (2007).

[3] Y. Lee et al., ACS nano, 9(2), 2061-2070. (2015).

[4] A. Mameli et al., ACS Applied Mater. & Interfaces 10, 38588-38595 (2018).

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