Atomic Layer Etching
Room Regency Ballroom A-C - Session ALE1-WeM

Integration & Application of ALE

Moderators: Bert Ellingboe, Dublin City University, Wei Tian, Applied Materials Inc.

8:00am **ALE1-WeM-1 ALD and Etch Synergy to Enable the Next Scaling Innovations***, **Angelique Raley**, K Lee, X Sun, Q Lou, Y Lu, M Edley, S Oyola-Reynoso, P Ventzek, R Clark, P Biolsi, H Masanobu, A Ranjan,* TEL Technology Center, America, LLC **INVITED**

As logic nodes continue to scale below 7 nm, the back-end-of-line (BEOL) critical pitch has moved to sub-40 nm and is forecasted to scale down to 14 nm according to the latest International Roadmap for Devices and System (IRDS). In addition to the patterning and integration complexities that arise with scaling, pitch reduction has a direct impact on the plasma-processing window. Conventional continuous wave processes can no longer achieve stringent aspect ratio dependent etching (ARDE), selectivity and profile control requirements and have gradually given way to pulsed plasma processes, decoupled process sequence plasmas or remote plasmas to widen the process space. In this talk, we will discuss implementation of atomic layer deposition (ALD) and decoupled or cyclic plasma etch in the BEOL to overcome challenges of mask loss, ARDE, low k damage and LER/LWR and look to future technology enablement with area and topographically selective processes.

ALD processes are achieved by using sequential, self-limiting reactions. ALD technology is widely used to go beyond lithography resolution limits, to increase selectivity and to enable self-alignment. For dielectric etches with fluorocarbon plasma chemistry a decoupled plasma etch process can achieve the benefits of an ARDE free etch with improved mask selectivity.

Integrations combining ALD and etch can yield further improvements in profile such as chamfer control and via CD control which have a direct impact on device reliability and yield. Finally, cyclic combinations of ALD and etch can drive down line width roughness through smoothing benefits of front growth merging and preferential etching of asperities.

8:30am **ALE1-WeM-3 On the Role of Individual Etching Components in Selective Atomic Layer Processing: Etch and Deposit to Obtain High Selectivity***, **Alfredo Mameli**,* TNO/Holst Center, Netherlands*; F Roozeboom,* Eindhoven University of Technology and TNO, Netherlands*; P Poodt,* TNO/Holst Center, Netherlands **INVITED**

In the domain of Atomic Layer Processing both Atomic Layer Etching (ALE) and area-selective Atomic Layer Deposition (ALD) are becoming increasingly popular because of their potential in advancing nanomanufacturing.[1, 2] Yet, the selectivity in terms of layer thickness and defectivity requirements has major limitations to overcome. Here, the combination of selective deposition and etching can play a key role in tackling these challenges.[3, 4] The complementarity of deposition and etching techniques offers great potential for reaching the targeted requirements for advanced applications.

In this presentation, the combination of spatial area-selective ALD using chemoselective inhibitors and interleaved etching steps to increase the process selectivity will be discussed. The focus will be on two different etching steps: the self-limiting etching of the inhibitor and a blanket etch-back step of the growing material. The former enables cyclic selective deposition when using a plasma-based ALD process while the latter allows for further maximizing the selectivity.

Finally, the concept of area-selective ALD combined with etching techniques in an integrated cyclic etch/dep spatial-tool for high-throughput Atomic Layer Processing will be presented.

[1] S. M. George *et al*, *ACS Nano*, **2016**, 10, 4889-4894

[2] A. Mameli *et al*, *ACS Nano*, **2017**, 11, 9303-9311

[3] K. J. Kanarik *et al*, *J. Phys. Chem. Lett.*, **2018**, 9, 4814-4821

[4] F. Roozeboom *et al*, *ECS J. Solid State Sci. Technol.*, **2015**, 4, N5067-N5076

9:00am **ALE1-WeM-5 Area-Selective Deposition of TiO_2 on Various Surfaces by Isothermal Integration of Thermal TiO_2 ALD and ALE***, **Seung Keun Song**, G Parsons,* North Carolina State University

As transistor size is shrinking, area selective deposition process is becoming more important than before. Atomic Layer Deposition (ALD) and Atomic Layer Etching (ALE) are promising processes for area selective deposition of metallic and dielectric materials as they can deposit and etch nanoscale thickness of thin film conformally. ALD precursors usually have different affinity to solid surfaces, which enables ALD processes to have surface dependent selectivity. For examples, thermal TiO_2 ALD, employing sequential doses of $TiCl_4$ and H_2O, shows initial growth delay on hydrogen-terminated silicon (Si-H) but rapid growth on oxide silicon surface (SiO_2) at 150-190°C. To extend this surface dependent selectivity, we created isothermal integrated ALD/ALE process, where TiO_2 ALD cycles are combined with a few cycles of thermal TiO_2 ALE, employing sequential doses of WF_6 and BCl_3, under isothermal condition. Using the integrated ALD/ALE sequence, we achieve ~ 7 nm of TiO_2 on SiO_2, before noticeable TiO_2 nucleation on Si-H, as determined by SEM, ellipsometry and TEM analysis. Process and materials analysis using in-situ QCM and ex-situ AFM and XPS further confirm our findings. Beyond TiO_2 selectivity on Si/SiO_2 surfaces, some metal surfaces (Cu, Au, Co) showed some extent of initial growth delay during TiO_2 ALD cycles, as observed by in-situ QCM. Thus, TiO_2 selectivity on various kinds of surfaces was also studied with ex-situ XPS, SEM, and ellipsometry. We expect that this demonstrated ALD/ALE process on various surfaces provides useful information about ALD/ALE precursors reactions on various surfaces, and this information offers opportunities to integrate ALD and ALE process with optimum process controls.

9:15am **ALE1-WeM-6 Limited Dose ALE and ALD Processes for Local Film Coatings on 3D Structures***, **Thomas Seidel**,* Seitek50*; M Current,* Current Scientific

The use of limited dose ALE and ALD are described for producing localized film coatings on 3D, non-planar structures such as trenches and fins. Limited dose ALD (LD-ALD) has been described for improved ALD film deposition rate (thickness/unit time)[1] and for local masking applications of DRAM bottle trenches.[2] In this paper we describe Limited Dose Atomic Layer Etch (LD-ALE) to obtain localized films on trenches and fins using various combinations of standard ALD, LD-ALD and LD-ALE. Three cases for localized film coatings are described:

(I) a film localized at the bottom of a trench or fin, by using standard ALD followed by LD-ALE,

(II) a film localized at the center of a trench or fin, using LD-ALD followed by LD-ALE, and

(III) a film localized at the top and bottom of a trench or fin, using ALD followed by LD-ALE, and this in turn followed by LD-ALD.

In case (I), the LD-ALE step is carried out using a prescribed limited ALE precursor modification[3] dose. The limited dose is prescribed to attain the desired local film etching and removal of a specified depth near the top of the non-local feature. As an application example, the local doping at the bottom of a bulk finFETs, is described using doped ALD films[4] at the bottom of a fin to counter dope the base of the fin. Separately, doping the source – drain region at the top of the fin is described. Examples of mask applications on trenches and fins will be described, as well as film localized thickness adjustments. Limited Dose implementation challenges as well as various equipment opportunities are briefly discussed. If experimental demonstrations are available, they will be presented.

1. G.Y. Kim et al, US 7,981,473, “Transient enhanced atomic layer deposition.”

2. T. Hecht, et al, US 7,344,953 B2, “Process for vertically patterning substrates in semiconductor process technology by means of nonconformal deposition.”

3. Lee, Y. et al., Chem. Mater. 28, 7657 (2016). Selectivity in Thermal Atomic Layer Etching Using Sequential, Self-Limiting Fluorination and Ligand-Exchange Reactions.”

4. A.U. Mane, et.al, "Atomic layer disposition of boron-containing films using B_2F_4", J. Vac. Technol. A34(1) (2016).

9:30am **ALE1-WeM-7 Formation of Ohmic Contacts to Si using In-situ Chemical Cleaning of the Substrate***, **Sara Iacopetti**,* Technion - Israel Institute of Technology, Israel*; R Tarafdar, S Lai, M Danek,* Lam Research Corp.*; M Eizenberg,* Technion - Israel Institute of Technology, Israel

The implementation of novel device geometries in CMOS technology such as FinFETs, allowed a further downscaling of the logic nodes to 45 nm and below, reaching nowadays mass production of devices of 7 nm and studies on sub-5 nm nodes. To such feature sizes and complex geometries, the well-established technology of Source and Drain (SD) contacts by metal silicide formation produces bulky contacts that cause short-channel effects,

detrimental to the transistor performances. Shallow ohmic contacts must be implemented in the future.

This work focuses on the feasibility of producing ohmic contacts using in-situ chemical cleaning (CC) of the native SiO_2 layer prior to the deposition of the contact metal (Co) without air break. The two main aspects investigated are the amount of Si consumption as a function of heat treatment, and the resultant contact resistivity.

Si blanket wafers were exposed to different number of cleaning cycles (increasing: No CC, CC-, CC+ and CC++); Co was deposited by PVD to isolate the effect of cleaning on the interface. Compositional and microstructural studies were carried by ToF-SIMS, XRD and HRTEM (STEM-EDS) on Si + 30 nm PVD Co, as-deposited and vacuum annealed. The CC removes completely the native oxide but creates a disordered interlayer of 2 nm thickness at the metal/semiconductor interface. Cobalt silicides formation is accelerated as a consequence of the removal of the native oxide, leading to the formation of a Co and Si intermixed layer from 200°C, and the onset of crystalline CoSi and $CoSi_2$ formation as early as 350°C and 450°C, respectively. As the resulting contacts are very thick (> 60 nm for the low thermal budget annealing), the approach to shallow contact fabrication moved to Si(CC) + PVD Co 10nm/TiN 30 nm/Co 200nm, without air break between depositions. The thin silicide formation with annealing of the contacts was checked by TEM and XRD and it follows the same silicide formation as seen in the Si + PVD Co 30nm case.

The contact resistivity was studied by fabrication of structures for transmission line measurement (TLM) by photolithography on Si/Co/TiN/Co, followed by wet or reactive ion etching of the metals. The contacts are ohmic and specific contact resistivities of 10^{-6} Ωcm^2 were measured, higher for the CC++ samples with respect to the non-cleaned and other cleaned samples, suggesting that the disordered interface plays a role as a thin dielectric barrier across the interface.

The ongoing research is focusing on the quantitative study of the interface composition and its influence on the contact resistivity, crucial for moving to an ALD metallization scheme.

9:45am **ALE1-WeM-8 SADP Spacer Profile Engineering by Quasi-Atomic Layer Etching**, ***Tsai Wen (Maggie) Sung***, *C Yan, H Chung, J Lo, D Desai, P Lembesis, R Pakulski, M Yang,* Mattson Technology, Inc.

As the size of modern device shrinks, self-aligned double patterning (SADP) and quadruple patterning (SAQP) has gained increasing interest in the fabrication of 14nm technology node and beyond. Plasma reactive ion etching (RIE) with inductively coupled plasma (ICP) is a common technique utilized in the SADP/SAQP process flow because of its etch anisotropy and tunability. Higher bias power is usually employed to achieve sufficient directionality; however, it can lead to sloped, sharp, and asymmetric spacer profiles. These undesired profiles may cause inadequate pattern transfer and the error may be amplified as it moves down the process line, such as pitch-walking and nonuniform fin formation. Furthermore, a high bias power can also severely damage the bottom substrate due to strong ion bombardment, resulting in an uneven etch. Recently, a method for quasi-atomic layer etching (QALE) was developed where it was found that the reactivity of a material increased with exposure to an active species.[1]

In this work, a chemical dry etch (CDE) equipment with an ICP radical source and a capacitively coupled plasma (CCP) plasma source was utilized to perform QALE. A RF bias was applied to the substrate to produce highly selective radicals and to promote vertical implantation of the active species into the top surface of SADP spacers. The implantation "activates" the spacer top surface by increasing its etch rate during a subsequent etch step, while keeping the etch rate of the unexposed sidewalls at a minimum, thereby improving the etch anisotropy. The activation-etch process is self-limiting and the etch depth scales linearly with the activation-etch cycles. By modulating this QALE method, we successfully demonstrated a significant reduction of the spacer shoulder slope and tip angle, thus flattened the spacer profile. Moreover, the QALE technique can be further developed and utilized to engineer the spacer surface profile and applied in other device fabrication processes.

[1]S.D. Sherpa and A. Ranjan, J. Vac. Sci. Technol. A **35**, 01A102 (2017).

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