ALD Applications
Room Grand Ballroom H-K - Session AA2-WeM
ALD for ULSI Applications I

Moderators: Ravindra Kanjolia, EMD Performance Materials, Han-Jin Lim, Samsung Electronics

10:45am **AA2-WeM-12 The Journey of ALD High-k Metal Gate from Research to High Volume Manufacturing**, ***Dina Triyoso**, R Clark, S Consiglio, K Tapily, C Wajda, G Leusink,* TEL Technology Center, America, LLC **INVITED**

In the early days of the search to find a replacement for SiO_2-based gate oxides the goal was to find a material with a very high k value which could be incorporated into CMOS production for multiple technology nodes. A historical overview of the many promising high k materials considered for SiO_2 replacement leading to the selection of ALD HfO_2 as "the winner" will be presented. ALD HfO_2 has successfully been implemented in CMOS production for over a decade, starting at the 45nm node. There are two general integration approaches for implementing ALD High-k/Metal Gate stacks (HKMG) in production: gate first and gate last. Challenges with each integration approach, leading to the wider adoption of gate last will be discussed. Furthermore, as the dielectric constant of HfO_2 is only ~20 and a thin SiO_2-base interface was still required to maintain mobility and reliability, HfO_2 provided essentially a one-time scaling benefit. Further thinning of HfO_2 resulted in unacceptable leakage and thus to continue transistor scaling fully depleted devices such as FINFET and Ultra Thin Planar SOI (FDSOI) were pursued. High volume manufacturing flows for FINFET (with gate last integration) and FDSOI (with gate first integration) come with their own unique challenges. For example, with FINFET maintaining gate height uniformity is crucial for Vt targeting and control. With FDSOI, maintaining gatestack stability at high temperature is key. To continue future scaling, new device architectures (e.g. GAA, Vertical FETs, etc.) will pose further challenges for gate stack integration. Recent and historical progress in HfO_2 growth, interface control, selective deposition, morphology and etching will be discussed with respect to the possibility for future gate stack engineering.

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11:15am **AA2-WeM-14 Effects of Er Doping on Structural and Electrical Properties of HfO_2 Grown by Atomic Layer Deposition.**, ***Soo Hwan Min**, B Park, C Lee,* Yonsei University, Republic of Korea*; W Noh,* Air Liquide Laboratories Korea, South Korea*; I Oh,* Yonsei University, Republic of Korea*; W Kim,* Hanyang University, Republic of Korea*; H Kim,* Yonsei University, Republic of Korea

Gate dielectric materials with high-*k* are required for further scaling down in future years. As an alternative of conventional high-*k* materials such as HfO_2, the addition of elements to host high-*k* materials has attracted attention. Among various elements, rare-earth elements, such as Y, La, Dy, or Er has been known to transform the crystal structure of HfO_2 from the first-principles study. The theoretical study showed that the doping into HfO_2 can energetically stabilize the cubic or tetragonal phase at lower temperature than thermodynamic conditions of pure HfO_2. Since cubic (*k*~29) or tetragonal (*k*~70) HfO_2 has much higher dielectric constant than that of amorphous (*k*~16-19) and monoclinic (*k*~20-25) phases, it is noteworthy that the structural modulation by doping of rare-earth elements can enhance the electrical properties of HfO_2.

In this work, Er doping into HfO_2 was experimentally carried out using atomic layer deposition (ALD) super-cycle process with $Er(MeCp)_2$(N-iPr-amd), $HfCl_4$, and H_2O co-reactant. ALD Er-doped HfO_2 with a variety of Er/(Er+Hf) compositions were systematically examined, mainly focusing on structural and electrical properties. X-ray photoelectron spectroscopy (XPS) and X-ray diffraction (XRD) were utilized to investigate the film composition and crystal structure. In addition, MOS capacitors were fabricated with various compositions to evaluate the electrical properties from capacitive-voltage (C-V) and current-voltage (I-V) measurements. In specific ratio, the dielectric constant and the interface trap density of Er-doped HfO_2 were found to have significantly improved compared to undoped HfO_2. Structural and electrical characterization revealed that the addition of Er to HfO_2 induces phase transformations from the monoclinic to the cubic or tetragonal phases, even at low post-annealing temperatures of 600°C. This study identifies optimum conditions to improve the electrical properties of Er-doped HfO_2 films which have potential applications in future nanoscale devices.

11:30am **AA2-WeM-15 Improvement of Electrical Performances of Atomic Layer Deposited ZrO_2 MIM Capacitors with Ru Bottom Electrode**, ***Jaehwan Lee**, B Park,* Yonsei University, Republic of Korea*; W Noh,* Air Liquide Laboratories Korea, South Korea*; I Oh,* Yonsei University, Republic of Korea*; W Kim,* Hanyang University, Republic of Korea*; H Kim,* Yonsei University, Republic of Korea

With accelerated scaling down and three-dimensional structuring of integrated circuits, it becomes very challenging to fabricate metal-insulator-metal (MIM) capacitors with low leakage current and high capacitance density. Specifically, the introduction of high-k dielectrics in conjunction with TiN electrodes has improved electrical properties in sub-100 nm processes. Various high-k dielectrics layers combined with TiN electrodes in MIM capacitors were studied for further improvement of MIM capacitors. Controlling an interfacial layer formation between dielectric layer and metal electrode is essential for depositing high-k dielectric thin film on a TiN electrode. When high-k dielectric films were placed on the TiN, interfacial layer was formed due to high reactivity of TiN. The interfacial layer acts as charge traps causing degradation of electrical properties. Surface treatment like plasma treatment on the TiN has been known to help suppress formation of an interfacial layer, but it would be hard to apply for mass-production of DRAM process due to difficulty of uniform treatment without damage caused by energetic species such as ions and radicals on the devices formed inside deep trenches with high aspect ratio.

Alternatively, selection of stable metal electrodes with high work function is required to improve electrical properties. Among several metals, Ru electrode can be appropriate option due to its good thermal and chemical stability, low resistivity, high work function. In this paper, we investigated effects of bottom electrodes on the thin film properties of atomic layer deposited (ALD) ZrO_2, concentrating on correlation between interfacial layer formation and electrical properties. Transmission electron microscopy (TEM) showed thinner thickness of the interfacial layer on the Ru electrode than TiN electrode. Chemical composition of the interfacial layer was analyzed by X-ray photoelectron spectroscopy (XPS) analysis, and ZrO_2 on Ru was less intermixed with bottom electrode due to good thermal and chemical stability of Ru electrode. Introducing Ru electrode improved symmetry of the normalized C-V characteristics. Simultaneously, the introduction of Ru electrode affects decrease of leakage current density from ~10^{-5} A/cm^2 to ~10^{-7} A/cm^2 in I-V characteristics. These results are very meaningful capacitor with Ru electrode can be a very promising device for MIM capacitor in DRAM production.

11:45am **AA2-WeM-16 Perfecting ALD-Y_2O_3/GaAs(001) Interface with Ultra-High Vacuum Annealing**, ***Keng-Yung Lin**, Y Lin, W Chen, H Wan, L Young,* National Taiwan University, Republic of China*; C Cheng,* National Chia-Yi University, Republic of China*; T Pi,* National Synchrotron Radiation Research Center, Republic of China*; J Kwo,* National Tsing Hua University, Republic of China*; M Hong,* National Taiwan University, Republic of China

High-performance metal-oxide-semiconductor field-effect transistors (MOSFETs) require the semiconductor/high-κ interface with high-temperature thermal stability and a low interfacial trap density (D_{it}). Previously, *in-situ* atomic layer deposition (ALD) or molecular beam epitaxy (MBE) Y_2O_3 has effectively passivated GaAs(001) surface.[1,2] The growth was achieved in an integrated ALD/MBE ultra-high vacuum (UHV) system. Despite the difference in deposition, both Y_2O_3/GaAs interfaces withstand 900 ^oC annealing, and the D_{it}'s lie below 5×10^{11} eV^{-1}cm^{-2}. MOS capacitors (MOSCAPs) with such interface outperform those with *ex-situ* deposited Al_2O_3.[3] By *in-situ* synchrotron radiation photoemission study on ALD-Y_2O_3/GaAs(001)-4×6, we found that the faulted surface As atoms were removed and lines of Ga-O-Y bonds stabilized the interface.[4] The interfacial Ga_2O (Ga^+)-like state explains the low D_{it}.

In this work, we have improved the electrical characteristics in ALD-Y_2O_3/GaAs by *in-situ* UHV annealing the initial 1-nm Y_2O_3. The idea is motivated by removing the freed As atoms and hydrocarbons remained in the ALD layer. Note that, an amount of hydrocarbons at such critical interface can degrade the device performances. ALD-Y_2O_3 was grown by thermal ALD with sequential $Y(EtCp)_3$ and H_2O pulses, and *in-situ* UHV annealing up to 600 ^oC was conducted in another chamber in our system right after the ALD growth. MBE-Y_2O_3 is relatively pure and employed as a reference.

Fig. 1 shows the capacitance-voltage (CV) and quasi-static CV (QSCV) curves for MOSCAPs. The UHV-annealed ALD-Y_2O_3/GaAs was improved with a reduced frequency dispersion (F.D.) in the accumulation/depletion region, and a lowered trap-induced hump in the inversion region. Fig. 2 presents the D_{it} spectra extracted from QSCVs. The UHV-annealed ALD-Y_2O_3/GaAs shows a reduced D_{it}, also hinted by the sharp transition of QSCVs and the narrow gap between QSCVs and CVs. Fig. 3 shows the O 1s core-level spectra, where O-Y is from the stoichiometric Y_2O_3 and O* is from the interfacial Ga-O-Y and the surface Y-O-H.[4] Note that the ratios of O-Y of our 1-nm Y_2O_3 films are significantly higher than the one reported.[5] Upon UHV annealing, the residue O* may be attributed to the interfacial Ga-O-Y with the surface Y-O-H mostly removed. This UHV annealing approach is significant in perfecting ALD-Y_2O_3/GaAs and is applicable to many other material systems.

References:

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