## ALD Applications
## Room Grand Ballroom H-K - Session AA2-WeA

### ALD for ULSI Applications II

**Moderators:** Iian Buchanan, Versum Materials, UK, Robert Clark, TEL Technology Center, America, LLC

**1:30pm AA2-WeA-1 Silicon-Based Low k Dielectric Materials with Remote Plasma ALD**, *Hyeongtag Jeon,* Hanyang University, Republic of Korea
**INVITED**

As the devices continue to shrink in size, resistive-capacitive (RC) time delay due to parasitic capacitance of devices is becoming a major problem. Low dielectric films with having high thermal stability and excellent step coverage is needed for applications such as barriers and gate sidewall spacers. Silicon oxycarbide (SiOC), silicon oxycarbonitride (SiOCN), silicon carbon nitride (SiCN) are possible candidates for these requirements because the carbon content and bonding state in the low dielectric materials can control the dielectric constant.

Atomic layer deposition (ALD) can be an ideal method for the high conformality with its self-limited reaction. The introduction of the plasma is necessary to decompose the ligands in the precursor for the ALD reaction by the plasma power. We used remote plasma ALD (RPALD) to prevent films from substrate damages caused ion bombardment.

In this work, we will discuss the trend of low k dielectric ALD studies and report the results of SiOC, SiOCN, and SiCN ALD. We used remote plasma ALD system. Octamethylcyclotetrasiloxane (OMCTS) and $O_2$, Ar, $H_2$, $N_2$ and $CH_4$+Ar plasmas were respectively used as a precursor and reactants for SiOC and SiOCN thin film deposition. Bis[(diethylaminohigh)dimethylsilyl](trimethylsilyl)-amine (DTDN-2) and $N_2$ plasma were used as a precursor and reactant for SiCN thin film deposition. X-ray photoelectron spectroscopy (XPS), Auger electron spectroscopy (AES), transmission electron microscopy (TEM), I-V measurement, C-V measurement, and wet etch rate (WER) test were performed for investigating the characteristics of low k dielectric films.

**2:00pm AA2-WeA-3 SiOC Films by PEALD with Excellent Conformality and Wet Etch Resistance**, *Young Chol Byun, E Shero,* ASM

As memory devices shrink, electrical and integration constraints have become tighter. As an example, digit line spacer stacks need to demonstrate a low dielectric constant (k<4.5), excellent wet etch rate resistance (an order of magnitude lower than thermal SiO2) and excellent conformality and growth over composite structures comprising a metal, hardmask and poly-Si. Conventional furnace-deposited ALD nitrides (SiN) tend to demonstrate good wet etch rate resistance but suffer high k (>7.0). PEALD oxides (SiO2) have a low-k but poor wet etch resistance and sub-optimal conformality on the composite stack due to the directional nature of the capactively-coupled plasma. But CCP plasma reactors typically offer higher throughput. This motivates the search for SiOC class of films to leverage Si-O bonding for low-k and Si-C bonding for step coverage, preferably deposited by PEALD.

Here, we demonstrate SiOC films with a low-k value (<4.5) with excellent step coverage and wet etch rate resistance due to Si-C backbonding (80X lower than furnace nitride and 500X lower than thermal oxide in hydrofluoric acid). The films also show good step coverage of 100% in upto 10:1 aspect ratio structures. In summary, these PEALD films show a pathway to aggressively scale k and wet etch resistance for front end memory applications.

**2:15pm AA2-WeA-4 ALD TiN for Superconducting Through-Silicon Vias**, *Kestutis Grigoras, S Simbierowicz, L Grönberg, J Govenius, V Vesterinen, M Prunnila, J Hassel,* VTT Technical Research Centre of Finland Ltd, Finland

Through-silicon vias (TSVs) are a widely used interconnect technique, allowing the creation of non-planar integrated circuits. Recently, the use of TSVs in multichip packages was proposed as a way of improving the addressability and integration of superconducting qubits – the core elements of superconducting quantum processors [1, 2]. In this approach, the primary quantum-coherent elements of a quantum integrated circuit can be separated from the readout and control elements by fabricating them on separate chips, which are then combined with flip-chip bonding. Here, routing signals through TSVs enables the addressability of a large number of qubits. The main requirements for TSV films are superconductivity, small dimensions, and conformality. To satisfy these challenging requirements, we use atomic layer deposition (ALD).

In this work, we investigate the performance of TiN TSV interconnects. We etch arrays of 60 µm diameter TSVs in 495 µm thick 6-inch silicon wafers by deep reactive ion etching using the Bosch process (Omega i2L, Aviza Technology). We use 2 µm thick oxide layers both as a mask (top side) as well as an etch stop layer (back side). We coat the TSVs with a TiN layer by ALD (SUNALE R-150B, Picosun), performing 2,500 cycles at 450°C, using $TiCl_4$ and ammonia as precursors and nitrogen as a carrier gas. The superconducting behaviour of thin TiN layers has been previously investigated for layers deposited by plasma-ALD [3], but this technique is not applicable for coating high-aspect-ratio trenches (the aspect ratio of our TSVs is about 8:1). Therefore, we use thermal ALD in this work.

Initially, the deposited layers did not become superconducting even at 0.1 K. Optimization of the ALD process by tuning precursor pulse/purge times finally led to superconducting TiN layers with a $T_c$ of approximately 0.85 K. The room temperature sheet resistance for a 47 nm thick layer is approximately 60 Ω/sq, as measured on the flat area of the samples. We confirm the conformality of the TiN inside vias using scanning electron microscopy. Future plans include increasing the $T_c$ as well as integrating TSVs on chips with other structures (resonators, qubits).

[1] Rosenberg et al., npj Quantum Information 42 (2017) 1-5.

[2] Vahidpour et al., arXiv:1708.02226 [https://arxiv.org/abs/1708.02226] [physics.app-ph].

[3] Shearrow et al., arXiv:1808.06009v1 [cond-mat.mtrl-sci]

**2:30pm AA2-WeA-5 Physical and Electronic Properties of Annealed ALD-deposited Ru from Ru(DMBD)(CO)$_3$ and Oxygen**, *Michael H. Hayes,* Oregon State University*; C Dezelah, J Woodruff,* EMD Performance Materials*; J Conley, Jr.,* Oregon State University

Ru metal is promising for MOS gate electrode and interconnect applications due to its relatively low bulk resistivity, high work-function, conductive oxide (RuO$_2$), and ease of etching. Because it is insoluble in and adheres well to Cu, Ru also has potential as a liner for metal interconnects. The earliest precursors used for ALD of Ru were often characterized by long nucleation delays (~200 cycles) and island-like growth, both unfavorable for producing uniform thin (< 10 nm) films. Recently, Austin et. al.[1] demonstrated a thermal ALD process using dimethylbutadiene Ru tricarbonyl [Ru(DMBD)(CO)$_3$] and O$_2$ that results in zero nucleation delay, low resistivity (14 µΩ-cm), and low RMS roughness (0.6 nm). While the resistivity is among the lowest reported, it is still higher than bulk crystalline Ru. In this work, we examine the impact of inert and forming gas anneals on the resistivity ($\rho_{Ru}$), effective workfunction ($\Phi_{Ru-eff}$) on ALD Al$_2$O$_3$ and HfO$_2$, crystal structure, and composition of ALD Ru films deposited using Ru(DMBD)(CO)$_3$ and O$_2$.

ALD Ru films of at least 30 nm in thickness are annealed at 400, 450, and 500 °C in either N$_2$ or 3% H$_2$/N$_2$ ambient in 20 minute increments up to a total of 60 min (Fig. 1). Whereas annealing in pure N$_2$ reduces $\rho_{Ru}$ from an average of 16 µΩ-cm to 13 µΩ-cm, H$_2$/N$_2$ annealing results in a greater reduction in resistivity with the lowest $\rho_{Ru}$ of 9.1 µΩ-cm obtained after 60 min at 500 °C, approaching the bulk value of 7.1 µΩ-cm. $\rho_{Ru}$ vs. Ru film thickness will be discussed at the meeting.

X-ray diffraction (Fig. 2) of the as-deposited films indicates hexagonal Ru with slight (001) preferred orientation and average crystallite size of 6.3 nm. After H$_2$/N$_2$ annealing, the relative intensity of the (001) peak is reduced and the crystallite size increased to 12.4 nm. Atomic force microscopy confirmed a slightly rougher film post anneal (2.1 nm RMS). XPS shows low impurity content.

Capacitance-voltage measurements are used to determine the flat-band voltage ($V_{FB}$) of a series of Ru/Al$_2$O$_3$/p-Si and Ru/HfO$_2$/p-Si MOS capacitors with various thickness ALD dielectrics for both as-deposited and 500 °C 60 min H$_2$/N$_2$ annealed samples. The extrapolated zero-oxide-thickness $V_{FB}$ was then used to determine $\Phi_{Ru-eff}$ for each dielectric (Fig. 3). Annealing increases $\Phi_{Ru-eff}$ to 4.9 eV and 5.3 eV for the Ru/Al$_2$O$_3$/p-Si and Ru/HfO$_2$/p-Si devices, respectively. Fast nucleation, low $\rho_{Ru}$ comparable to bulk, and large $\Phi_{Ru-eff}$ comparable to sputtered films indicate ALD Ru using Ru(DMBD) and O$_2$ may offer advantages compared to previous reports.

[1] D. Z. Austin *et al.*, "ALD of Ru and RuO$_2$ Using a Zero-Oxidation State Precursor," *Chem. Mater.* 29(3), 1107 (2017).

**2:45pm AA2-WeA-6 Fluorine Free Boron-Containing Composite Layers for Shallow Dopant Source Applications**, *Anil Mane, D Choudhury, K Pupek, R Langeslay, M Delferro, J Elam,* Argonne National Laboratory

Conformal and uniform coatings of boron-containing thin films via atomic layer deposition (ALD) could be used as a shallow dopant source for

advanced 3D-transistor structures in VLSI manufacturing. Targeting this application, we evaluated three non-halogenated boron compounds for their suitability as ALD precursors: boric acid ($B(OH)_3$), trimethyl borate ($B(OCH_3)_3$), and hafnium borohydride $Hf(BH_4)_4$. The $B(OH)_3$ and $B(OCH_3)_3$ were used in combination with trimethyl aluminum to deposit $B_xAl_{2-x}O_3$ ALD films, and the $Hf(BH_4)_4$ was used with $H_2O$ to deposit $HfB_xO_y$ films. We evaluated the ALD surface chemistries for these processes using in-situ quartz crystal microbalance (QCM) and Fourier transform infrared spectroscopy (FTIR) studies. The QCM measurements also confirmed self-limiting behavior and helped to optimize the ALD timing. The resultant boron containing nanocomposite films were analyzed using X-ray photoelectron spectroscopy (XPS), secondary ion mass spectrometry (SIMS), ellipsometry, and electrical capacitance measurements. The boron content in the $B_xAl_{2-x}O_3$ and $HfB_xO_y$ composite films was controllable by tuning the ALD cycle ratio and the precursor sequence. We performed rapid thermal annealing of composite films as a function of time and temperature and determined the B-diffusion in silicon as well as changes in the optical properties of the $B_xAl_{2-x}O_3$ and $HfB_xO_y$ layers. Here we will present a detailed investigation of ALD methods for creating B-containing layer for shallow dopant application.

### 3:00pm AA2-WeA-7 Impact of Medium Energy Ions on the Microstructure and Physical Properties of TiN Thin Layers Grown by Plasma Enhanced Atomic Layer Deposition (PE-ALD)., *S Belahcen, C Vallée, A Bsiesy, Marceline Bonvalot,* LTM-UGA, France

Titanium nitride TiN has been extensively used in common microelectronic devices as an electrode material, where it serves as an interfacial connecting material between a device and the metallic contacts used to drive it, while simultaneously preventing any diffusion of the metal into silicon. TiN is also involved in biological Micro-Electro-Mechanical Systems (bioMEMS) as an electrode material, for instance in cardiac pacemakers or neural stimulation applications, thanks to its unequalled conducting properties at reduced dimensions, as compared to traditional noble metals, and also thanks to its high corrosion resistance to human body fluids. For such applications, a deep knowledge of the microstructural properties of TiN are of utmost importance.

In this work, the impact of processing parameters on the physical properties of TiN has been investigated in details. TiN thin layers (20 nm) have been prepared on $SiO_2$ (100 nm)/Si substrates by Plasma Enhanced ALD (PE-ALD), using TDMAT as a precursor and $N_2$ as a plasma gaz. The PE-ALD setup used for this purpose has been equipped with an original Atomic Layer Etching (ALE) kit positionned at the back-face of the substrate holder, which allows medium energy ions to be extracted from the plasma during the ALD growth. Several bias values ranging from 0 W to 90 W have thus been tested during the plasma step to investigate the impact of ions with varying kinetic energies on the morphological properties of TiN.

The rugosity of as deposited TiN layers has been obtained from AFM measurements. XRD and XRR analyses have been systematically carried out in order to evaluate the texturation, cristallinity and mechanical stress in the layer. The impact of medium energy ions during TiN growth has been correlated to the rugosity, density and residual stress. These results will be discussed in view of potential applications of TiN as an electrode material in microelectronic devices.

### 3:15pm AA2-WeA-8 ALD Process Monitoring for 3D Device Structures, *Jiangtao Hu,* Lam Research Corp.

Semiconductor device structures have become increasingly complex, requiring new measurement techniques to support manufacturing. Measurement of high aspect ratio (HAR) structures requires a response signal to depth and profile, and the bottom may be invisible to top-down optical signals. Likewise, certain thick films are opaque to optical thickness measurement. Lateral processing steps occur too deeply in a structure to be visible, and thin conformal deposition films need to be characterized inside the feature.

For ALD applications, a critical requirement is to have complete and uniform coverage from the top to the bottom of a 3D device. A thinner or incomplete deposition at the bottom of a device can often lead to high leakage and high failure rates. Conventional optical thickness measurements of ALD films can identify thickness variations at the top of a high aspect ratio (HAR) device but may not identify process deviations at the bottom of this type of device.

Monitoring ALD using mass metrology is a potential solution to this issue. The direct measurement of mass change due to process enables detection of process excursions. Measurement of the wafer mass before and after a process is a simple and direct means of monitoring and control. This is

particularly true for ultra- opaque films and complex stacks, film density monitoring, and conformal and ALD/sidewall deposition, where traditional optical metrology techniques may not be effective.

Conformal deposition typically involves an area much greater than a blanket deposition layer, and even more so on severe/strong/high device topologies. Mass sensitivity to film on a patterned wafer can be as much as 10 times greater than on a blanket wafer (Fig 1).

More importantly, mass metrology directly monitors the amount of material change in a device across the entire HAR structure while conventional optical film metrology typically measures these changes on a test pad or blanket test wafer. Mass metrology instrumentation can detect low coverage of ALD films at the bottom of a HAR device which otherwise would be missed using optical measurement. For example, we can compare mass change induced by flow rate reduction on blanket or patterned wafers (Fig 2). Significant mass change occurs on patterned wafers after a 3% of flow rate reduction, while on patterned wafers this deviation is pronounced after a 1% reduction.

In this discussion, we will discuss how Mass Metrology can be used to monitor ALD process variations in 3D semiconductor devices, along with the applications and benefits of this technology in ALD.

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