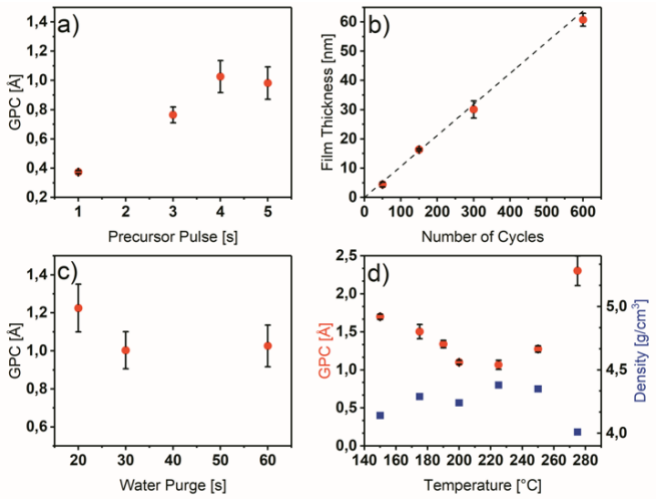

Figure 1. (a) Precursor saturation studies by the variation of the [Y(DPDMG)$_3$] pulse length at 225 C on Si(100). (b) Film thickness versus number of applied cycles. (c) GPC variation with water purge time at 225 C on Si(100). (d) GPC and thin film density as a function of deposition temperature.

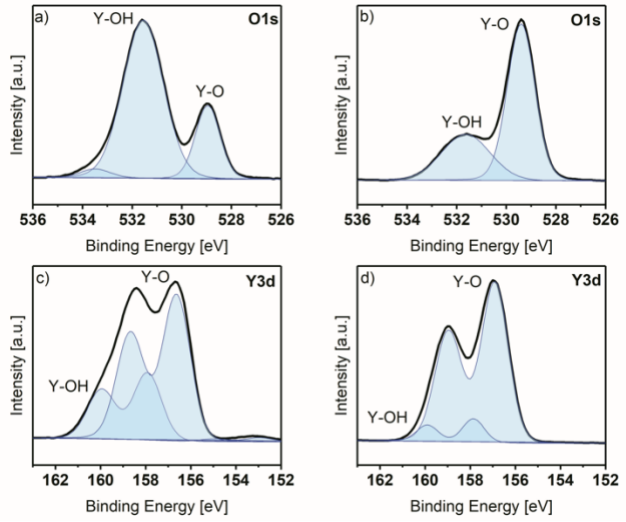

Figure 2. XPS O1s and Y3d core level spectra of the thin film deposited at 225 °C (30 nm). a) Normalized O1s peak as-introduced. b) Normalized O1s peak after sputtering. c) Normalized Y3d peak as-introduced. d) Normalized Y3d peak after sputtering. Blue curve: Fitted regions for different core contributions. Black curve: Measured data.

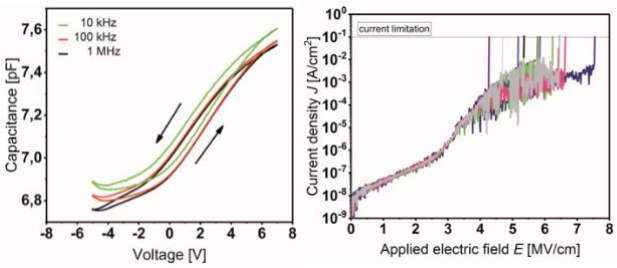

Figure 3. Left: Capacitance-voltage curves of Y_2O_3 based MIS capacitors for f = 10 kHz, 100 kHz and 1 MHz. The 20 nm Y_2O_3 thin film was deposited at 200 °C. Right: Leakage current density J as a function of the applied electric field E of several MIS capacitors incorporating Y_2O_3. Each color represents a J–E characteristic of an individual device with identical device geometries. The 20 nm Y_2O_3 thin-film was deposited at 200 °C.

[1] L. Mai, N. Boysen, E. Subasi, T. de los Arcos, D. Rogalla, G. Grundmeier, C. Bock, H.-L. Lu, A. Devi, *RSC Adv.*, 2018, **8**, 4987.