ALD Applications
Room 116-118 - Session AA1-MoA

Memory Device & Materials I

Moderators: Steven M. George, University of Colorado at Boulder, Christophe Vallee, LTM - MINATEC - CEA/LETI, France

1:30pm **AA1-MoA-1 Atomic Layer Deposition as a Key Technology for Manufacturing 3D V-NAND Flash Memory**, ***Jaeyoung Ahn***, Samsung Electronics, South Korea*; J Jee, P Nam, B Kim, J Yang, D Kim, H Choi,* Samsung Electronics **INVITED**

The introduction of 3D V-NAND enables the high capacity, fast processing storage solutions to implement the emerging technologies such as cloud computing, big data, internet of things and mobile devices. Since the memory array size of 3D V-NAND has been increasing over the years, it is inevitable to stack more cells vertically, which builds stumbling blocks in deposition of various materials on the cell structures. ALD has been successfully adopted in the process integration as the key technology for CTF dielectric layers, gap-filling dielectrics, and word-line metals due to its superior step coverage and uniformity. However, since the surface area of the structures is expanding rapidly, it is very challenging to maintain good step coverage and uniformity for future generations of 3D V-NAND. During the process flow of 64-stacked V-NAND Flash devices, patterned wafers frequently show over 30 times larger surface area compared to blanket wafers and very high vertical and lateral aspect ratios. Consequently, we need advanced technologies employing new hardware platforms, more efficient precursors, and optimized process conditions. At the same time, we also need selection criteria to identify the right solution for each ALD step in the process flow. For these purposes, we propose numerical simulation of mass transfer using computational fluid dynamics approach as a tool for developing advanced ALD hardware and materials as well as optimizing existing processes.

2:00pm **AA1-MoA-3 Room-temperature Resonant Tunneling by Band-offset Engineering of Nanolaminated High-k Oxides Deposited by Atomic-layer Deposition**, ***Hector Uribe-Vargas***, *J Molina-Reyes,* National Institute of Astrophysics, Optics and Electronics

Due to the continuous scaling of advanced CMOS technology, high-k oxides became very important due to a low leakage current and high dielectric constant (k>8). These oxides are often deposited by atomic-layer deposition (ALD), which has a high reproducibility, conformality, outstanding control (to atomic level) on the thickness and stoichiometry and a low deposition temperature (T≤250°C). Because of these characteristics and taking advantage of the band offsets between silicon and different high-k oxides, a double barrier resonant tunneling (RT) diode could be formed. In this regard, RT devices have shown promise at achieving very high speed in wide-band devices and circuits that are beyond conventional transistor technology, nevertheless, this effect is often seen in highly complex crystalline heterostructures (usually fabricated by epitaxial growth), and only at very low temperatures (T<77 K).

In this work, 2 sets of 2 samples of metal-insulator-insulator-insulator-semiconductor (MIIIS) devices were fabricated. The first set of 2 samples is a stack of ultra-thin Al_2O_3, HfO_2 and Al_2O_3 (AHA stack with 2nm, 1nm and 2nm in thickness) deposited by ALD. After gate deposition, one sample was subjected to post metallization annealing (PMA) at 450°C for 30 minutes in an H_2/N_2 ambient. For the second set of 2 samples, a stack of ultra-thin Al_2O_3, TiO_2 and Al_2O_3 (ATA stack with 2nm, 1nm and 2nm in thickness) was also deposited by ALD and similarly, one sample was also subjected to PMA. These devices were designed in order to promote quantum-well (QW) formation at the intermediate oxide layer, having QW of 1.3 eV and 3.1 eV respectively and promoting RT conduction during substrate injection of electrons.

After Ig-Vg measurements at room temperature, experimental proof of RT via negative differential resistance (NDR) was demonstrated in MIIIS structures fabricated using ALD, putting this deposition technique as a powerful tool to obtain this phenomena after atomic control of all high-k layers. Due to the difference in the band gaps of different high-k materials, it is possible to promote quantization of discrete energy levels in intermediate layers of stacked ultra-thin high-k oxides. For the case of the AHA ($Al_2O_3/HfO_2/Al_2O_3$) structure, 3 distinctive NDR zones are observed after substrate injection. For the case of the ATA ($Al_2O_3/TiO_2/Al_2O_3$) structure, even though no evident NDR is present, RT is a strong possibility due to a high non-linearity (~20), high asymmetry and low dynamic resistance. When PMA is performed, no sign of RT/NDR is obtained in both AHA and ATA structures, due to an inner diffusion of atomic elements within the stacked oxides.

2:15pm **AA1-MoA-4 Atomic Layer Deposition of HfO_2 Thin Films using $Hf(BH_4)_4$ and H_2O**, ***Devika Choudhury***, *A Mane, R Langesley, M Delferro, J Elam,* Argonne National Laboratory

High dielectric constant (high-k) metal oxides and their silicates have been extensively studied as alternatives to SiO_2 for electronic and optoelectronic applications [1]. Excellent dielectric properties coupled with high thermal stability has made HfO_2 one of the most popular replacements for SiO_2 in CMOS and DRAM devices. HfO_2 thin films have been deposited using various methods including CVD, ALD, sputtering, and sol-gel techniques [2]. However, with the decreasing size of devices and increasing demand for ultrathin conformal films with precise thickness and composition control, ALD has emerged as the preferred method.

ALD of HfO_2 has so far been successfully implemented using different precursors. $HfCl_4$ and HfI_2 are two of the most commonly used Hf sources, which however require high deposition temperatures (>300°C) and generate corrosive byproducts (HCl and HI). Although alternative precursors like metalorganics or amides have also been used, the possibility of carbon contamination has restricted their use in electronic applications [3].

In this work, we demonstrate the relatively low temperature ALD of HfO_2 thin films using a carbon free precursor, tetrakis(tetrahydroborato)hafnium [$Hf(BH_4)_4$], and H_2O. As both precursors have substantial vapor pressure at room temperature, low temperature deposition growth is possible. Self-limiting, linear growth of HfO_2 is obtained at 200°C, and experiments on the feasibility of lower temperatures deposition are underway. The refractive index of the as-grown films measured at 632 nm is found to be 1.91, which indicates the formation of HfO_2. Stronger confirmation for HfO_2 is obtained by elemental analysis using X-ray photoelectron spectroscopy (XPS). The doublet of the Hf 4f orbital electrons obtained at binding energies of 18.4 and 20.1eV can be assigned to the Hf $4_{7/2}$ and Hf $4_{5/2}$ electronic states of Hf in Hf-O bonds respectively. Moreover, the O1s peak obtained observed at 531.9eV also corresponds to formation of Hf-O bonds in the as-deposited film. XRD analysis showed the films deposited at 200°C to be amorphous, but rapid thermal annealing at 750°C for 60s yields crystalline, monoclinic HfO_2 films.

References:

[1] E.P. Gusev, C. Cabral Jr., M. Copel, C. D'Emic and M. Gribelyuk; Microelectronic Engineering 69 (2003) 145–151.

[2] K. Kukli, M. Ritala, T. Sajavaara, J. Keinonen and M. Leskela; Thin Solid Films 416 (2002) 72–79.

[3] K. Kukli, M. Ritala, J. Sundqvist, J. Aarik, J. Lu, T. Sajavaara, A. Harsta and M. Leskela, Journal of Applied Physics; 92 (2002) 5698-5703.

2:30pm **AA1-MoA-5 TaN Based Multi-Vth Devices for 7nm and Beyond Technology**, ***Donghun Kang***, *T Abrams, V Chhabra, S Han, H Parvaneh, B Kannan, G Xu, R Lu, M Ozbek, S Krishnamurthy, P Mennell, H Wang, J Liu,* GLOBALFOUNDRIES U.S. Inc.

Multiple Vth (Multi-Vth) have been one of key components in RMG to meet different industry demands. To extend it to future technologies, several issues need to be resolved; lowering nFET Vth, developing etching process and mitigating TaN loading at different macros. In this study, we demonstrated TaN based multiple Vth devices with 12% better Toxgl adopting higher Al contained nFET work function, selective TiN etching and improved TaN micro-loading.

Fig.1 illustrated simplified process flow in RMG area. Etch of TiN/TaN stack were carried out by using different chemistries (Fig2). Chemistry A removes completely both TiN and 99% of TaN, which is good one for none-selective etching. On the other hand, other chemistries show reasonable selectivity with TaN, which could be a potential selective TiN removal process. Among them, chemistry D is chosen for the selective removal, considering RIE effect on TaN etching rate in Fig.3

Micro-loading was evaluated at three locations, flat, short channel and long channel regions. Each location has its own unique physical structure and surrounds, which could influence source population. Fig.4 compares deposited TaN thickness with different TaN deposition conditions. Significant loading (short/long channel thickness, >50%) was observed from control process. To compensate geometry effect, precursor flow, pule and purge time have increased, expecting better delivery to FIN in trench. With this approaches, loading short to long channel dramatically reduces to 15% in Fig. 4.

Fig.5 and Fig 6 summarize key device results. In Fig 5, both high Al conditions can lower nFET Vth than that of baseline process, demonstrating the ability to push nVTh down further. Fig. 6 shows the benefit of Toxgl for different Al content devices. High Al conditions achieves around 12% better Toxgl than control due to high K protection by TaN during patterning process. TaN based multi-Vth has successfully demonstrated with resolving, 1) nFET Vth lowering by higher Al content in NWF, 2) development/optimization of selective and none-selective etch, and 3) improvement in TaN micro-loading associated with physical shapes of macros. Higher Al nWF process is very effective to lower nFET Vth with matching device parameters. Improved source delivery is a key factor to reduce micro-loading up to 15%. Toxgl benefit of 12% has confirmed by better HfOx protection from patterning process.

2:45pm **AA1-MoA-6 Atomic Layer Deposition: A Few Prospective Applications Aiming Mass-production after Current Si-based Semiconductor Process**, ***Tae Joo Park,*** Hanyang University, Republic of Korea **INVITED**

ALD (atomic layer deposition) is one of the most advanced thin film coating or deposition technique in the current vacuum science or electronic device fabrication processes. Recently, the matured ALD technique begins to look for new applications with its strong advantages such as the superior step coverage (conformality) on complicated 3D structures and extremely-precise film thickness controllability. Up to now, there have been a few feasible applications of ALD technique aiming at mass production; electrical and chemical passivation of the assorted solar cells and organic/inorganic flat panel displays, of which fabrication process and physics are familiar with those of semiconductor devices.

This presentation starts with the introduction of modified/advanced ALD process for current Si based industry; discrete feeding method (DFM) and electric field-assisted ALD (EA-ALD) technique for efficient metal film growth to achieve ultrathin and continuous thin film. Next, new-type 2-dimensional electron gas (2DEG) field-effect transistor comprised of only two ALD binary oxide films and wafer-scale uniform ALD growth of 2D chalcogenides will be introduced as part of post-CMOS technology. ALD applications for energy system are also briefly discussed such as Li-based composite thin films for secondary batteries and catalytic/protective layer for photoelectrochemical cells. Another important application of ALD technique could be the design of core-shell structured nano/micro particles for multifunctional applications. A specially designed ALD reactor enables the successful fabrication of core-shell structured nano/micro particles irrespective of the chemical reaction conditions (pH, temperature etc). This technique is also applicable to passivation of various quantum dots and microparts.

3:15pm **AA1-MoA-8 Atomic Layer Deposition of NbO_x Films with Tunable Stoichiometry Using Hydrogen Plasma Reduction**, ***Alexander Kozen,*** *T Larrabee, M Twigg, H Cho, S Prokes,* U.S. Naval Research Laboratory

The Niobium oxide system has seen recent interest, particularly due to its potential use as both a non-volatile, in the case of Nb_2O_5, or volatile, in the case of NbO_2, memristor material. Nb_2O_5 is a high k dielectric (k~41) with a high refractive index (n~2.2) and a wide bandgap (3.6 eV), while NbO_2 is a thermochromic material that undergoes a first order crystalline phase transition at a critical temperature (T_c) of 800˚C. Both of these phases, along with their intermediate sub-oxides, can serve as material components of memristors to facilitate low-power neural computing hardware.

Using the same metalorganic precursor, $^tBuN=Nb(NEt_2)_3$, we demonstrate deposition of NbOx films containing tunable ratios of Nb^{4+} and Nb^{5+} by incorporating additional H_2 plasma steps into the ALD process to selectively reduce Nb^{5+} atoms to a lower oxidation state. The ability to produce NbOx thin films with specific metal to oxygen ratios is critical to understanding the memristive switching behavior of the NbOx materials system, while use of one chemical precursor to deposit a spectrum of varying material stoichiometry and phase can greatly simplify fabrication and design of neuromorphic circuits.

We will examine the impact of plasma chemistry, number, and duration of both single and multiple H_2 plasma steps in the Nb_2O_5 ALD process on film growth, chemistry, and morphology, and will discuss how these additional steps can be used to reduce the resulting film from pure phase amorphous Nb_2O_5 to a NbO_2-rich amorphous film. Additionally, we elucidate the relationship between overall film stoichiometry and electrical properties, with a focus on memristive switching behavior of these materials.

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