Plenary Session
Room Plaza ABC - Session PS1-SuM

Sunday Plenary Session I

Moderators: John Conley, Oregon State University, Charles Dezelah, EMD Performance Materials

8:30am **PS1-SuM-3 Future Applications and Challenges for ALD in Microelectronics**, ***Suvi Haukka***, ASM, Finland **INVITED**

The number of different materials in semiconductor devices has been increasing nearly exponentially with the down-scaling of device dimensions. For decades the device consisted of mainly Si based materials, but by the late 1990´s it became clear these materials alone cannot enable the required scaling. Furthermore, the deposition methods used were unable to meet the ever more stringent requirements. Thus atomic layer deposition (ALD), although considered too slow at that time, started gaining increasing interest. ALD dielectrics were the first to be investigated, especially due to the need for ultra-thin and highly conformal films. In early 2000 first ALD Al2O3 and later ZrO2 were used in memory applications, while in 2007 ALD HfO2 replaced SiO2 as the gate oxide in transistors at the 45 nm node. Now ten years later the research community is facing even greater challenges in future device scaling, which calls for new ALD processes, or even completely new deposition methods. We all working in the deposition field are challenged to deposit high quality materials at low temperatures, such as low resistivity metals and patterning layers. Also we are requested to deposit many materials selectively only on certain surfaces, for instance to overcome lithography misalignment issues. Since there is less and less room for all the different layers, the thickness of each layer is approaching 1nm or less making the uniform deposition demanding. Furthermore, the materials should also be deposited conformally in extremely high aspect ratio, highly complicated and very high surface area structures. These industry needs drive new materials requirements which put great demands on the ALD chemistry. It is essential to understand the chemistry of the starting surfaces, interfaces and the interaction of precursors with the varying surfaces to make it possible to selectively deposit uniform and continuous layers less than 1 nm thick. Any of the challenges mentioned could be difficult to overcome, unless we understand in detail how to design and optimize our ALD reactors for the new chemistries. Thus not only the chemistry of ALD, but also the hardware play a big role in how successful we will be. In this presentation the various future applications and challenges are reviewed with the main focus on how the ALD chemistry is critical for developing solutions.

9:15am **PS1-SuM-6 Future Trends of Deposition Technologies in Semiconductor Industry**, ***Mei Chang***, Applied Materials **INVITED**

3D transistor FinFET, 3D memory, and multiple patterning have been driving the semiconductor industry for the recent years. While Moore's Law is still on going, dimensional scaling has slowed down noticeably; instead, the focus has shifted toward stacking vertically. The challenges to deposit films conformally and to fill the features free of void are getting more severe. On top of them, the demand for various functional materials is continuously expanding on the periodic table.

In this talk, we will discuss several technologies: thin conformal coatings, void free filling, and selective deposition; their application and tradeoffs.

Plenary Session
Room Plaza ABC - Session PS2-SuM

Sunday Plenary Session II

Moderators: Steven M. George, University of Colorado at Boulder, Keren J. Kanarik, Lam Research Corp.

10:45am **PS2-SuM-12 Atomic Layer Etching – An Overview of Possibilities and Limitations**, ***Richard Gottscho***, Lam Research Corp. **INVITED**

Exceeding expectations set back in the 1980s, today the field of plasma etching is more critical than ever to formation of nanometer-sized features in a $35-40 billion chip equipment industry. For most critical etch applications such as pattern-transfer and 3D structure formation, an essential requirement is the anisotropic removal of material. Plasma is important because it provides the energetic, directional ions that enable anisotropy, while also producing radicals to accelerate reactions. Conventional plasma etching was for many years considered a "black box" of coupled non-linear interactions between ions and radicals [1]. Atomic layer etching (ALE) is an advanced etch technique used in the fabrication of 10 nm logic. By virtue of its separated and self-limiting steps, ALE offers a simplified system in which to understand etch mechanisms. In this talk, we'll explore plasma ALE focusing on silicon ALE as a case study before expanding the concepts and applying them to a variety of other materials relevant to the industry such as Ge, C, W, GaN, and SiO_2 [2, 3]. A "synergy" parameter quantifies the degree to which each process approaches the ideal ALE regime and is related to the energetics of underlying surface interactions. By systematically studying a group of materials, we show that synergy scales with surface binding energy of the bulk material. This helps explain why some materials are inherently more (or less) amenable to the ALE approach. The insights will be vital for exploiting ALE in the fabrication of future devices.

[1] H.F. Winters, J.W. Coburn, E. Kay, J. Appl. Phys. 48, 4973 (1977)

[2] K.J. Kanarik et al., J. Vac. Sci. Technol. A 33(2), Mar/Apr 2015

[3] K.J.Kanarik et al, J. Vac. Sci. Technol. Submitted Dec 2016

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