Tuesday Afternoon, July 18, 2017

ALD Applications
Room Plaza E - Session AA2-TuA

ULSI, High-k and III-V I (1:30-3:30 pm)/ULSI, High-k and III-V II (4:00-5:00 pm)

Moderators: Scott Clendenning, Intel Corporation, Elton Graungard, Boise State University, Sven Van Elshocht, IMEC

1:30pm **AA2-TuA-1 ALD as an Enabler of Self-aligned Multiple Patterning Schemes***, **Sven Van Elshocht**, Z Tao, J Everaert, S Demuynck, E Altamirano-Sanchez,* IMEC, Belgium **INVITED**

Dimensional scaling is since many decades one of the main drivers of technological advancement. It is captured in what is often referred to as Moore's law: a doubling of the number of transistors every ~2 years for the same cost. The last couple of years this trend has been slowing down, but is still very much alive.

One of the main issues is the difficulty to keep printing ever smaller features in a well-controlled and reliable matter. While smaller wavelength lithography tools are not yet into mass production, alternative techniques are being used to extend the current 193nm litho capability.

As an alternative to single exposure, multipatterning techniques are employed. One approach is multiple litho-etch (LE), where the litho print is divided into multiple partial prints that together form the targeted image. The pattern can as such be split in for example 2 or 3 prints, i.e. LELE or LELELE. The biggest concern with this method is overlay or the alignment of the different partial prints to each other.

To circumvent the problem of overlay, one has implemented self-aligned multiple patterning (SAMP). The first print forms a pattern on which a conformal spacer is deposited. After removal of the first material, referred to as the core or mandrel, one obtains a pattern with twice the density and where the width of the features is determined by the deposited spacer thickness. This procedure can be multiple times and result in double or quadruple patterning schemes.

In this presentation, we will demonstrate that Atomic Layer Deposition (ALD) is highly suited to fulfill the requirements as spacer deposition technique for SAMP. In addition, we will discuss the requirements of patterning materials in general toward. As a concrete example we will discuss fin patterning for a 7-nm logic technology node using Self Aligned Quadruple Patterning (SAQP).

2:00pm **AA2-TuA-3 Thin Film Dopant Sources Grown by PALD for Shallow Semiconductor Doping***, **Bodo Kalkofen**, M Silinskas,* Otto von Guericke University, Germany*; M Lisker,* IHP GmbH, Leibniz-Institut für Innovative Mikroelektronik*; Y Kim,* Lam Research Corporation

Plasma-assisted atomic layer deposition (PALD) was carried out for growing thin oxide films containing dopants for silicon, germanium, and SiGe. The applicability of these films as dopant sources for shallow doping of those semiconductor materials using various rapid thermal annealing methods, such as RTP, flash lamp and laser annealing, was investigated. Remote conductively coupled plasma and inductively coupled plasma sources were applied for generating oxygen radicals in the PALD processes. Tris(dimethylamido)borane was used as boron containing precursor for p type doping, source layers for n type doping were grown using triethylphosphite and triethylantimony for phosphorus and antimony containing oxides, respectively.

The as-deposited films of boron oxide were highly unstable in ambient air and could be protected by capping with in-situ PALD grown antimony oxide films. Phosphorus containing films were stabilized by incorporating them into a silicon dioxide matrix by carrying out ALD processes with supercycles of phosphorus and silicon precursor reactions with oxygen radicals. Also capping of the phosphorus containing films was applied. Antimony oxide films were stable at ambient air conditions.

Boron and phosphorus doping of Si could be obtained using the respective oxide films as dopant sources. This was confirmed by SIMS and sheet resistance measurements. A phosphorus dopant level >1E20 cm^{-3} in silicon could be formed with ALD doping and short time annealing by laser or flash, while a level of >1E19 cm^{-3} was obtained with RTP (950 °C) annealing. Diffusion of antimony into SiGe and Ge from antimony oxide could be shown. The influence of source layer thickness and different annealing conditions during rapid thermal annealing processes on the doping results was investigated.

2:15pm **AA2-TuA-4 Effective Work-Function of PEALD Metal Nitrides and its Tuning by Co-deposition***, **Ekaterina Zoubenko**, I Krylov, B Pokroy, M Eizenberg,* Technion - Israel Institute of Technology, Israel

The implementation of nitride based metallic compounds (e.g. TiN, WN) as metal gate materials is attractive for complimentary metal-oxide-semiconductor (CMOS) applications. Tuning the effective work-function (EWF) is challenging. The effective work-function of metal nitride has a wide range of values and depends on the dielectric material, the metal microstructure and its chemical composition. Recently, plasma enhanced atomic layer deposition (PEALD) at high vacuum (10^{-6}torr) using amid-based metalorganic precursors has enabled the deposition of low resistivity metal nitrides. The ALD technique, which is based on self-limiting surface reactions, enables the co-deposition of various metals and provides an additional degree of freedom to EWF engineering. However this issue was not investigated systematically in literature.

In the current work, EWF on SiO_2 of pure metal nitrides (TiN, WN, TaN and MoN) is presented. In addition, EWF tuning by metal nitride alloying at various compositions (e.g. TiN+WN) and its evolution with thermal annealing temperature will be discussed. The thickness, microstructure, chemical composition and electrical resistivity of the films were determined by X-ray reflectivity (XRR), X-ray diffraction (XRD) and transmission electron microscopy (TEM), X-ray photoelectron spectroscopy (XPS) and four-point probe (4PP), respectively. The EWF of metal nitrides on SiO_2, using MOS structure, was studied using capacitance-voltage (CV) measurements and plotting the flat-band voltage (V_{FB}) versus the effective oxide thickness (EOT).

As an example, as deposited TiN films of 30[nm] have poly-crystalline FCC structure, as determined by XRD and TEM. XPS depth profiling indicated carbon and oxygen concentrations of 3at%, which leads to a low value of resistivity of 110 [μΩ·cm]. The EWF of TiN on SiO_2 was determined to be 4.6±0.1 [eV], namely that the position of Fermi level is close to Si midgap. This combined with the low resistivity make TiN a good candidate for CMOS applications. Similar systematic study will be presented for other metal nitrides and their alloys.

2:30pm **AA2-TuA-5 Surface Morphology, Crystallinity and Electrical Properties of Some Rare-earth Oxide ALD Films***, **Satu Ek**, R Ritasalo,* Picosun Oy, Finland*; T Sarnet,* Picosun Oy*; J Kalliomaki,* Picosun Oy, Finland*; E Østreng,* Picosun Oy*; S Vangelista, A Lamperti, S Spiga,* CNR-IMM - MDM Laboratory*; R Piagge, G Ghidini,* STMicroelectronics

Rare-earth oxides (REOs) have interesting optical and electrical properties that make them useful for several applications. Many REOs have high dielectric constant (k), which can easily reach values k > 20. Therefore, they are relevant for the microelectronics industry. At present, there is a growing need for thinner gate dielectrics of current materials, such as SiO_2, which might lead high leakage currents, subsequently leading to increased power dissipation, reliability problems and unaccepted electrical breakdown [1,2]. The implementation of high-k gate dielectrics is one of several strategies developed to allow further miniaturization of microelectronic components. A possible gate dielectric material needs to fulfill certain requirements [1]: (i) k-value high enough to fulfill the roadmap of components scaling, (ii) thermodynamically stable with Si, (iii) kinetically stable, and compatible with processing to 1000°C for few seconds, (iv) act as an insulator, by having band offsets with Si of over 1eV to minimize carrier injection into its bands, (v) form a good electrical interface with Si, and (vi) have few bulk electrically active defects.

In this work, we have succeeded in the deposition of various REOs, such as CeO_2, La_2O_3,Y_2O_3, and Y_2O_3-doped Al_2O_3 (Y:Al_2O_3), in a uniform manner on 200mm Si wafers using a Picosun R-200 Advanced atomic layer deposition (ALD) reactor. REO films were deposited using $Ce(thd)_4$, $La(thd)_3$ and $Y(thd)_3$ as metal-containing precursors, and ozone as oxidizer.

The surface morphology, crystallinity and grain size of the deposited layers were studied. Conformality maps, AFM surface morphology and XRD analysis of Y_2O_3 and Y:Al_2O_3 films are presented in Fig. 1 as an example. The results show that uniform ALD layers were deposited, i.e. 1.4-2.5% (1σ non-uniformity), with a very smooth surface, with 0.5 nm roughness. Additionally, electrical measurements of the REO films were studied. Fig. 2 shows an example of the effect of Y_2O_3 content in Al_2O_3 on the breakdown field and leakage current. The Y_2O_3 films exhibit a high dielectric breakdown field (>6 MV/cm), a relatively high k value (~11), and a low-leakage current density (<10^{-8} A/cm^2at 3 MV/cm) with 100nm layer deposited at 300 °C, well-comparable to the values obtained by de Rouffignac et al. [2]. By adjusting the amount of Y_2O_3 in Al_2O_3 a good

compromise can be reached with relatively high growth rate, low leakage and high breakdown together with relatively high k-value.

[1] Robertson, Eur. Phys. J. Appl. Phys. 28 (2004) 265–291.

[2] de Rouffignac et al., Chem. Mater., 17 (19) (2005) 4808-4814.

Acknowledgements: This work received funding from TEKES and ECSEL-JU R2POWER300.

2:45pm **AA2-TuA-6 Atomic Layer Deposition of High-k Oxide Films from La(NO$_{33}$·6H$_2$O Solution Oxidant**, ***In-Sung Park**, S Kim, T Lee, S Seong, Y Jung, J Ahn,* Hanyang University, Republic of Korea*; J An, J Yun,* Korea Research Institute of Standard and Science (KRISS), Korea

High-k films have been widely applied on the gate dielectric, capacitor dielectric, insulator in resistive memory, and even optical layer. ALD is a leading method in the formation of ultrathin layer of nm scale and the uniform/conformal coating on the complex substrate structure. In the fabrication of binary metal oxide films, the complete cycle of ALD typically consists of four steps: (1) pulsing with metal precursor; (2) purging with inert gas; (3) pulsing with oxidant; and (4) purging with inert gas.

In the ALD of metal oxide, the choice of both metal precursor and oxidant is very important for a successful ALD process. Various oxidants have been reported such as H_2O, O_3, and plasma-O_2 for the fabrication of metal oxide films. The oxidant can change the characteristics of the deposited oxide films such as crystalline structure, growth rate, and electrical properties. In this work, the high-k metal oxide films of ZrO_2 and HfO_2 were synthesized by using atomic layer deposition method with $La(NO_3)_3{\cdot}6H_2O$ solution as oxygen source. The high-k oxide films formed with $La(NO_3)_3{\cdot}6H_2O$ have been investigated by comparing the films formed with H_2O oxidant on the material and electrical properties.

Several findings are highlighted by the alternative introduction of $La(NO_3)_3{\cdot}6H_2O$ solution to H_2O.

La elements in the deposited high-k films are not detected using the X-ray photoelectron spectroscopy, meaning La plays like a catalyst during ALD process.

The introduction of $La(NO_3)_3{\cdot}6H_2O$ solution effectively altered the crystalline structure, grain size, and surface roughness of the grown high-k films. For example [1], the crystalline structure of the ZrO_2 film changed from a mixture of tetragonal and monoclinic phases to monoclinic phase. The average grain size is doubled from 140 nm to 200-280 nm by using $La(NO_3)_3{\cdot}6H_2O$ solution, and the resulting film surface became rougher.

However, the concentration of $La(NO_3)_3{\cdot}6H_2O$ solution had little influence on the above crystalline properties.. The average grain sizes of the ZrO_2 films prepared from $La(NO_3)_3{\cdot}6H_2O$ solution at concentrations of 10, 20, 30, and 40% were 280, 256, 208, and 200 nm, respectively.

Considering the relation between optical bandgap energy and crystalline properties of high-k films, the controlled properties of crystalline films using $La(NO_3)_3{\cdot}6H_2O$ solution contribute to the optical and electrical devices.

[1] N. K. Oh et al., Applied Surface Science 394, 231 (2017).

3:00pm **AA2-TuA-7 Great Enhancement of Dielectric Constant via High Temperature Annealing ALD Bi-layered Oxides**, ***Keng-Yung Lin**, L Young, C Cheng, Y Lin, H Wan,* National Taiwan University, Republic of China*; R Cai, S Lo,* Industrial Technology Research Institute, Republic of China*; M Hong,* National Taiwan University, Republic of China*; J Kwo,* National Tsing Hua University, Republic of China

To push the high-speed, low-power device performances beyond Si-based MOSFETs, incorporating high-mobility GaAs as the channel material onto Si wafers is a promising way. Moreover, by utilizing high dielectric constant (k) oxides as the gate stacks, enhanced drain current is expected by capacitance effective thickness (CET) scaling, without the severe gate leakage caused by tunneling. Thus, enhancement of the dielectric constant in the high-k/GaAs system is vitally important. In this work, we have *in-situ* deposited atomic-layer-deposited (ALD) Y_2O_3(2.3nm)/Al_2O_3(5.0nm) and HfO_2(1nm)/HfAlO(9nm) bilayers respectively on freshly grown molecular beam epitaxy GaAs(001), followed by *ex-situ* post-deposition rapid thermal annealing and top/back gate electrodes formation. The dielectric constants of the gate stacks and the high-k/GaAs interfaces are characterized by conventional frequency-dependent capacitance-voltage (C-V) measurements. The k value of the Y_2O_3/Al_2O_3 bilayer increased from 11.1 to 15.6, a 40% enhancement, for the 900°C-annealed sample, compared to that of the as-deposited one. Note that the thicknesses of the oxide films have been verified by scanning transmission electron microscopy (STEM). The interfacial electrical characteristics between Y_2O_3/Al_2O_3 and GaAs also significantly improved by having smaller frequency dispersion in accumulation/depletion region as shown in Fig.1. We have also discovered a dielectric constant enhancement for HfO_2/HfAlO on GaAs. We have used an initial HfO_2 layer to prevent direct inter-mixing between Al_2O_3 and GaAs, which was known to degrade the CV characteristics during high temperature annealing. After annealing over 850°C in helium ambience, the dielectric constant increased from 17.6 to 22, a 25% enhancement, as shown in Fig.2. In addition, the frequency dispersion at accumulation region was reduced from 18.3% to 10.7%, indicating a lower interfacial trap densities (D_{it}) and high thermal stability at the HfO_2/GaAs(001) interface. In summary, we have greatly increased dielectric constant of ALD oxides in Y_2O_3/Al_2O_3 and HfO_2/HfAlO bilayers by mixing them via a thermal approach. Note that no new phases formed, as were studied using high-resolution synchrotron radiation X-ray diffraction and STEM (Fig.3). The high temperature annealed high-k/GaAs(001) interfaces are significantly improved, showing excellent thermal stability. The method for the formation of high quality mixed high-k materials could be generic for other ALD bi-layered oxides for future applications.

†K. Y. Lin and L. B. Young have made equal contributions to this work.

* M. Hong and J. Kwo are the corresponding authors.

3:15pm **AA2-TuA-8 Atomic Layer Deposition of Novel Interface Layers on III-V Channel Devices**, *F Tang, **Xiaoqiang Jiang**,* ASM*; Q Xie,* ASM, Belgium*; M Givens,* ASM*; J Maes,* ASM, Belgium*; S Sioncke, I Tsvetan, L Nyns, D Lin, N Collaert,* IMEC, Belgium

III-V compound semiconductors are considered promising transistor channel materials to enable further scaling beyond Si technology due to their high bulk electron mobility values. However, unlike Si, III-V materials have poor quality oxides, and high-k dielectric deposited directly on the III-V surface is problematic due to high density of interface states (D_{it}) and oxide traps. A surface treatment is typically required to passivate the semiconductor surface to minimize the interface states. In addition, a deposited interface layer (IL) is required for the integration with high-k dielectrics to reduce the impact of oxide traps while maintaining a low D_{it}. Although extensive study has been done on searching appropriate IL, commonly investigated high-k metal oxides appear limited in ability to meet the performance requirements for a robust III-V channel transistor.

In this work, a thermal ALD process of a novel material is demonstrated for application as IL in III-V channel devices. The IL material is deposited using a commercially available, hot walled cross flow reactor (ASM Pulsar 3000®). Saturated thickness is demonstrated over a wide range of pulse times in Fig. 1(a) and (b), indicative of operation in the ALD regime. The growth per cycle of is 0.23Å shown in Fig. 1(c). The $In_{0.53}Ga_{0.47}As$ MOSCAPs demonstrate superior D_{it} values <$1x10^{12}$ $cm^{-2}eV^{-1}$, low accumulation dispersion (<1%), and hysteresis (<30 mV) values, extracted from CV characteristic as shown in Fig 1(d). The device performance matches previously published benchmark device metrics for InGaAs channel devices [1]. By employing this novel IL, high performance InGaAs nanowire MOSFETs built on 300 mm silicon wafers is also demonstrated with transconductance reaching 2200 [2].

To further improve the hysteresis or reliability of device, a secondary lanthanum silicate ($La_xSi_{1-x}O$) IL is introduced prior to the deposition of HfO_2 high-k. This lanthanum silicate is deposited by a H_2O-based ALD processes. An ALD master cycle includes a lanthanum oxide sub cycle and silicon oxide sub cycle, shown in Fig. 2(a). Fig. 2(b) shows the growth per master cycle and [Si] content extracted from RI values of bulk films. By using novel IL/lanthanum silicate IL/HfO_2 gate stack, the InGaAs MOSFET demonstrates an excellent electron mobility with a reduced oxide traps meeting the reliability target for 10 years operation [3].

In a summary, we developed novel ALD films for IL application, yielding excellent electrical properties on III-V devices.

[1] M. Radosavljevic et al., IEDM Tech. Dig., 765 (2011)

[2] N. Waldron et al. IEDM Tech. Dig., pp 31.1 (2015)

[3] S. Sioncke et al. submitted to VLSI (2017)

4:00pm **AA2-TuA-11 ZrO_2 as a High-k Gate Dielectric for Enhancement-mode AlGaN/GaN MOS HEMTs**, ***Charles R. Eddy, Jr.**, V Wheeler,* U.S. Naval Research Laboratory*; D Shahin,* University of Maryland*; T Anderson, M Tadjer, A Koehler, K Hobart,* U.S. Naval Research Laboratory*; A Christou,* University of Maryland*; F Kub,* U.S. Naval Research Laboratory

Advanced applications of AlGaN/GaN high-electron-mobility transistors (HEMTs) in high-power RF and power switching are driving the need for an insulated gate technology. We present here basic and early applied studies

of the use of zirconium oxide (ZrO_2) as a high-k, high breakdown gate dielectric for reduced gate leakage and a fully-recessed barrier structure for enhancement-mode operation of AlGaN/GaN HEMTs. We include the study of GaN surface preparations for dielectric deposition, surface/interface characterization and device operation wherein a world record threshold voltage of +3.99V is achieved.

An optimum GaN surface preparation involving a piranha etch followed by a thermal oxidation of the surface has previously been shown [1] to result in smooth, clean GaN surfaces that exhibit the best electrical performance when ALD high-k dielectrics are deposited thereon. This same preparation is applied to ALD ZrO_2 dielectrics. ZrO_2 films were deposited by atomic layer deposition (ALD) using two different metal precursors [zirconium (IV) tert-butoxide (ZTB) and tetrakis(dimethylamido)zirconium(IV) (TDMAZ)] and water. For the former we also assessed both water and ozone as the oxygen precursor. ZrO_2 films grown by ALD with ZTB were found to be slightly oxygen rich whether ozone or water were used as the oxygen source. However, films grown with ZTB and ozone did have carbon contamination. Films grown with TDMAZ and water were found to be stoichiometric and free of carbon.

Films grown with ZTB and water on optimally prepared surfaces again shown the best electrical performance for the dielectric-semiconductor interface in terms of smoothness, low leakage in forward and reverse bias (< 10^{-5} A cm^{-2}) and low hysteresis. Unlike in previous studies with ALD deposited Al_2O_3 and HfO_2, where total trapped charge was in the mid-10^{11} to low 10^{12} cm^{-2} range, ZrO_2 films show considerably higher trapped charge densities in the high 10^{12} to mid-10^{13} cm^{-2} range. The nature of this charge is uncertain at this time but believed to be due to excess oxygen in ZTB deposited films and is directly responsible for a 1.5 – 2 V positive shift in threshold voltage.

[1] C.R. English, et al., J. Vac. Sci. & Technol. B 32,03D106 (1-17) (2014).

4:15pm **AA2-TuA-12 Investigation of High-quality Silicon Nitride (SiN_x) Thin Film Grown by Low-temperature Hollow Cathode Plasma-Enhanced ALD as a Gate Dielectric for AlGaN/GaN MIS-HEMTs**, ***Xin Meng**, Y Byun, J Lee, H Kim, J Lee, A Lucero, L Cheng, J Kim,* University of Texas at Dallas

AlGaN/GaN metal-insulator-semiconductor high electron mobility transistors (AlGaN/GaN MIS-HEMTs) have been studied for power device applications. To mitigate current collapse and address the instability in threshold voltage (V_{th}), silicon nitride (SiN_x) has been widely investigated as a gate dielectric and passivation layer. This attributes to the low density of SiN_x/III-N interface states, achieved by passivating the defects related with nitrogen-vacancy and suppressing the formation of interface traps related with the Ga-O bonds. Recently, AlGaN/GaN MIS-HEMTs using a PEALD SiN_x gate dielectric have shown improved device performance [1]. Nevertheless, the film properties of the low-temperature SiN_x employed in these studies (SiH_4/N_2 plasma: low refractive index 1.7-1.85 and low density ~2.5 g/cm^3) cannot compete with those of the high-quality films grown by a high-temperature CVD process (e.g. MOCVD or LPCVD).

In this work, we report AlGaN/GaN MIS-HEMTs using high-quality PEALD SiN_x as the gate dielectric. SiN_x was deposited at a calibrated wafer temperature of 310 °C (16 nm,1500 cycles, set temp. 400 °C) in a home-made ALD system equipped with a Meaglow™ hollow cathode plasma source (Figure 1). Tris(dimethylamino)silane (TDMAS or 3DMAS) and N_2 plasma were used. High-quality SiN_x films were obtained (e.g., high refractive index 2.0, high mass density 2.9 g/cm^3, very low wet etch rate 0.8 nm/min in 100:1 dilute HF, dielectric constant ~7, and high breakdown electric field 11 MV/cm). *Ex-situ* XPS analysis showed a low oxygen content (2 at. %) and a negligible carbon content (<1 at. %) in the bulk film. Growth per cycle (GPC) was approximately 0.11 Å/cycle. The AlGaN/GaN MIS-HEMTs (L_{SG}=4.5 μm, L_G=5 μm, L_{GD}=6.5 μm, V_{DS}=10 V) showed a maximum drain current ~550 mA/mm, a high on/off ratio 10^9, a large gate bias swing, and a steep subthreshold swing of 72 mV/dec. Furthermore, negligible V_{th} shift and a small hysteresis (~ 100 mV) were observed between forward and reverse sweep under a large gate bias ($V_{G,\ max}$= 10 V), as shown in Figure 2. The excellent stability of V_{th} indicated fewer interface/border traps near the dielectric/III-N interface. The capacitance-voltage characteristics also showed a negligible hysteresis (Figure 3) and small frequency dispersion. A detailed comparison with Schottky barrier HEMTs and thermal ALD Al_2O_3 MIS-HEMTs will be presented. Our work has demonstrated that PEALD is a suitable technique to grow high-quality SiN_x film for AlGaN/GaN MIS-HEMTs applications.

[1]. X. Meng et al., "Atomic Layer Deposition of Silicon Nitride Thin Films: A Review of Recent Progress, Challenges, and Outlooks," Materials, 9 (12), 1007 (2016)

4:30pm **AA2-TuA-13 Atomic Layer Annealing for Atomic Layer Epitaxy of AlN Ultrathin Films at a Low Growth Temperature**, *M Chen, **Wei-Hao Lee**, H Shih, W Kao, Y Chuang,* National Taiwan University, Taiwan*; R Lin,* Chang Gung University, Taiwan*; H Lin,* National Taiwan University, Taiwan*; M Shiojiri,* Kyoto Institute of Technology, Japan

Atomic layer deposition (ALD) is an attractive technique for preparing high-quality nanoscale thin films, and has been widely exploited in a great variety of nanoscale applications including solar cells, memories, and transistors. However, the as-deposited thin films prepared by ALD are generally of amorphous-like structure due to the requirement of a low deposition temperature to keep the self-limiting chemical reactions in ALD. As compared with amorphous films, crystalline films or even single-crystalline epitaxial layers are more favored because of the significantly improved optical and electrical properties. Therefore, it is highly demanded to improve the crystallization of the ALD-deposited thin films. In this work, a novel concept and approach termed as "atomic layer annealing" (ALA) was proposed in the ALD process to realize the low-temperature atomic layer epitaxy, i.e., to achieve high-quality epitaxial growth of AlN at a low deposition temperature of 300°C on sapphire substrate. Rather than a high growth temperature which is needed in conventional epitaxial growth techniques, a layer-by-layer, in-situ Ar plasma treatment was introduced into each ALD cycle to realize the ALA effect. The Ar plasma treatment during each ALD cycle provides sufficient crystallization energy to the surface of thin films from the incident radicals or ions, leading to the dramatic transformation of the AlN ultrathin film from the amorphous phase to a single-crystalline epitaxial layer. The X-ray diffraction and high-resolution transmission electron microscopy clearly indicates a high-quality single-crystal AlN epilayer with only a few tens of nanometer in thickness. In addition, the two-dimensional electron gas (2DEG) characteristic of the AlN/GaN heterojunction was also observed by the ALA treatment on the AlN layer. The result demonstrates great potential for further extension of the ALD tools from the conventional deposition of amorphous thin films to high-quality epitaxial growth at a low temperature, which can be utilized in a variety of fields and applications in the near future.

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